A High-Efficiency High-Power-Density On-Board Low-Voltage DC-DC Converter for Electric Vehicles (EVs) Application

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Abstract: On-board low-voltage dc-dc converter (LDC) in electric vehicles is used to connect the high voltage battery with the low voltage auxiliary system. With the advancement of auxiliary equipment in electric vehicles (EVs), the output current of the LDC can be hundreds of amperes, which will cause high conduction loss and severe thermal concern. In this paper, a high-efficiency high-power-density on-board LDC is presented. To reduce current stress and improve efficiency, three phase interleaved LLC dc-dc converters are paralleled to provide 270A load current. Synchronous rectifier (SR) is used to reduce secondary conduction loss. ZVS turn-on of primary switches and ZCS turn-off of secondary switches are achieved, thus switching loss can be reduced significantly. Moreover, phase-shedding technology is used to improve light load efficiency. Switch-controlled capacitor (SCC) technology is used to achieve accurate load current sharing among the three phases, which protects the devices against high current stress, reduces the conduction loss and improves the reliability of the system. As SCC switches achieve ZVS turn-on and turn-off by its nature, the loss of the SCC circuit is of less concern with regard to the rated output power. In addition, GaN HEMTs are used in the primary side to improve the power-density and eventually help achieving light weight. A 3.8kW (14V/270A) LDC prototype is developed and tested. Experimental results show good current balancing among the three phases. A peak efficiency of 96.7% at 140A load, and a full load efficiency of 95.8% are achieved with 3kW/L power-density and 1.5kg weight.

Keywords—Electric vehicles (EVs), LLC dc-dc converter, Synchronous rectifier, Switch-controlled capacitor

I. INTRODUCTION

With increasing environmental pollution caused by greenhouse gas emissions from conventional fossil fuel-driven vehicles, electric vehicles (EVs) are attracting increasing attention as they are not only more environmentally friendly, but cheaper than fossil fuels vehicles [1]. Along with the development of electric vehicles (EVs), more and more auxiliary equipment, e.g. air conditioning, is required to satisfy consumer requirements. High power on-board low-voltage dc-dc converter (LDC) is essential in electric vehicles (EVs), which takes responsibility to transfer power from high-voltage battery to auxiliary equipment and low-voltage battery. As shown in Fig. 1, the battery system of EVs consists of high voltage (HV) Li-ion batteries (250V to 430V) and low voltage (LV) Lead-acid batteries (9V~16V). In general, HV batteries are used for traction of motor drives. LV batteries provide power for auxiliary equipment. As more and more auxiliary equipment is implemented in EVs to provide various additional features nowadays, such as lighting, audio/video systems, air conditioners, automatic seats, sunroofs, heated seats, etc., high load current level of LDC is the trend. From [1]-[2], at least 2.4kW power rating is required to supply auxiliary equipment. Therefore, the LDC should output more than 200A load at 12V.

Typically, EVs charger system operates at two modes, 1) the HV battery is charged from the grid by the off-board charger or the on-board charger when the vehicle is connected to the grid. 2) the HV battery provides power to auxiliary electronic devices or charges the LV battery through LDC when the vehicle is running [1]. In general, the voltage range of HV battery and LV battery system is wide. Galvanically isolated dc-dc converters are required in LDC to ensure safety and obtain high step-down voltage ratio (430V to 9V). Moreover, high power density and light weight are desirable for LDC due to the limitation on space and weight for EVs. Last but not least, high efficiency is required to extend the mileage per charge and to reduce the heatsink size.

In [1], phase-shift full bridge converter is adopted in LDC. However, it is difficult to achieve ZVS for the lagging arm under light load. To guarantee ZVS of primary switches in LDC based on phase-shift full bridge converter, auxiliary inductors are used in [2]-[4]. In [5], a built-in buck circuit is used in transformer secondary of LDC to solve the induced voltage caused by the multi-winding high-frequency transformer.

In [1]-[7], phase-shift full bridge converter is adopted for LDC, and current-doubler circuit is utilized in the transformer secondary to provide high load current [1]-[3], [6]. However, compared to a phase-shift full bridge dc-dc converter, resonant
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converter such as LLC dc-dc converter benefits from that ZVS of primary switches and ZCS of secondary switches can be achieved, which is used widely in various application to achieve high-efficiency and high power-density [8]-[13].

In [14]-[17], LLC dc-dc converter is adopted in LDC of EVs. As output current is high in LDC, transformer secondary conduction loss is predominant. Thus, the efficiency could be improved significantly by using synchronous rectifier (SR) LLC dc-dc converter in [14]-[15]. To reduce transformer secondary current stress, two phase interleaved LLC dc-dc converter is used, and phase shedding technology is adopted to improve light load efficiency in [16]. [17] utilizes both LLC and B/DCM control schemes to improve efficiency and power-density.

Multi-phase dc-dc converters connected in parallel can help reduce the current stress, which makes an effective way to improve the efficiency. However, for the LDC based on LLC resonant converter, when switching frequency is close to series resonant frequency, the impedance of $L_r$ and $C_r$ in series is close to zero. Small tolerance on $L_r$ or $C_r$ will cause large impedance difference among different phases, thus the load current would be unbalanced severely and induce uneven heating of the circuit components. If current sharing cannot be achieved in multi-phase resonant dc-dc converters connected in parallel, one of the phases may carry all the output current and the other phases may carry no output current. This will degrade the efficiency, increase the current stress and even damage the board. Therefore, current sharing problem needs to be solved to improve the efficiency and reliability.

In [16], two separate voltage loop controllers are utilized in two-phase LLC dc-dc converters connected in parallel, which makes two phase current sharing by operating two phases at the different switching frequency. However, the different switching frequencies will cause beat frequency, which deteriorates the performance of the converter. In [18], two extra auxiliary PWM dc-dc converters are used to make two-phase LLC-DCX input current sharing. By transforming the current sharing of the resonant converter into PWM control of a dc-dc converter, this method is simple to implement. However, to make sure that the PWM converter only processes small partial power, the components tolerance of two DCX should be very small.

Current sharing can also be achieved by using series connection in multi-phase LLC converter with small resonant components tolerance [19]-[23]. Moreover, three-phase LLC dc-dc converter with Y connection or Δ connection is also confirmed to achieve current sharing by series connection [21]-[23]. However, a serious current imbalance still occurs if large resonant component tolerance presents in three-phase LLC dc-dc converter. In addition, all three phases need to operate at the same time even with light load, thus, the light load efficiency will be degraded.

Compared to multi-phase LLC dc-dc converters connected in parallel directly, RMS input voltage of the resonant tank is lower in three-phase LLC dc-dc converter with Y connection or Δ connection. The current stress of primary components in three-phase LLC dc-dc converter with Y connection or Δ connection is higher under the same specification and the number of switches, which increases conduction loss. Therefore, multi-phase LLC dc-dc converters connected in parallel have the following advantages: 1) low current stress can reduce the conduction loss; 2) unneeded phases can be shut down to improve the efficiency in light load condition.

To implement current sharing in multi-phase LLC dc-dc converters connected in parallel with the same switching frequency, several methods have been proposed in [24]-[30]. By adding capacitors, inductors, etc. passive impedance network so that the impedance of the resonant tanks are matched, good performance of current sharing is achieved in [24]-[27]. In [28]-[30], magnetic-coupling is adopted to achieve three phases current sharing. However, to achieve good current sharing performance, all these methods [21]-[30] required small resonant components tolerance. Otherwise, these methods will become ineffective.

Switch-controlled-capacitor (SCC) method is proposed in [31] to modify the resonant capacitor value so that resonant components tolerance can be compensated and current sharing among phases can be obtained. In [32]-[35], SCC technology has been verified in resonant dc-dc converter to achieve current sharing. Compared with conventional current sharing approaches, SCC technology can achieve current sharing accurately even under large tolerance among phases.

This paper proposes a high-efficiency and high-power-density LDC in EVs application by using a three-phase interleaved LLC dc-dc converter. The novelty of the proposed LDC lies in 1) reducing the current stress and conduction loss by the proper LDC circuit configuration design; 2) SCC circuit is used and current sharing accurately is achieved in three phase LLC dc-dc converters at the same switching frequency even when the three phase converters have large resonant components tolerance; 3) the phase-shedding capability is realized to improve light load efficiency. Therefore, high efficiency of wide operating range and high power-density are very promising in the proposed LDC, which benefits from balanced and low current stress, phase shedding capability, soft switching of switches in LLC converter and SCC circuit, low conduction loss of the SCC circuit switches by using the novel modulation strategy, and GaN HEMTs are used as primary side switches.

In this paper, Section II illustrates the circuit configuration and conduction loss analysis. Current sharing technology is given in Section III. Section IV presents the parameters selection of the resonant components, and Section V gives the optimal design of the LDC. Experimental results and conclusion are given in Sections VI and VII.

II. ANALYSIS OF THE LDC CONFIGURATION

According to the specification of the proposed LDC, the full load current is 270A at 14V output. If single-phase LLC converter is used as shown in Fig. 2, 270A load current would flow through SR switches $S_1$ and $S_2$. The conduction loss on the secondary side would be prohibitively high.

Fig. 2. Single-phase LLC converter
To reduce the transformer secondary conduction loss, [17] and [36] propose the circuit configuration that using four transformers with series-input parallel-output to reduce the current stress of transformer secondary, as shown in Fig. 3. However, only one phase full bridge inverter and resonant components are used in transformer primary, conduction loss would also be large at heavy load.

Instead of using one phase on the transformer primary side, several phases parallel connection topology can be used to provide high load current. Taking three phase parallel connection as an example, each LLC converter needs to provide 90A out of 270A load current, as shown in Fig. 4. Thus, each transformer needs to process only 45A load current.

![Fig. 3. Single-phase LLC converter with 4 transformers series-input parallel-output in [17] and [36]](image)

Based on the above assumption, the comparison of the RMS current and copper loss are given in Table I at $V_{in}=380V$, $V_o=14V$ and $I_o=270A$. For the convenience of the comparison, several assumptions are made in Table I, i.e., the on-state resistance of SRs is $R_{d,SR}=0.5\, m\Omega$, the on-state resistance of primary switches is $R_{d,OP}=100m\Omega$, the resistance of transformer primary is $R_{Tx,p}=65m\Omega$, the resistance of transformer secondary is $R_{Tx,s}=1.5m\Omega$ and the equivalent series resistance of inductor $L_r$ is $R_{in}=75m\Omega$. Core loss and switching loss are not considered as they do not change too much with the current.

According to Table I, the transformer primary currents stress of the circuits in Fig. 2 and Fig. 3 are three times of that in Fig. 4; and the transformer secondary current stress of the circuit in Fig. 2 is six times that in Fig. 4. As the conduction loss is related to the square of RMS current, the copper loss and conduction loss of the circuit in Fig. 4 are reduced significantly.

Compared to the three phase converters shown in Fig. 4, the single phase topology in Fig. 2 produces 124.1W extra loss, which will cause 3.3% efficiency degrading at 14V and 270A output and bring difficulty to the cooling system.

To reduce conduction loss and improve efficiency, the proposed LDC for EVs adopts three phase interleaved LLC dc-dc structure. Moreover, two transformers with input-series output-parallel are used in each phase LLC dc-dc converter to further reduce the secondary side SR conduction loss.

### Table I: Comparison of Loss in Different Full Bridge LLC DC-DC Converter Structure

<table>
<thead>
<tr>
<th>Structure</th>
<th>1 modular in Fig. 2</th>
<th>1 modular in Fig. 3</th>
<th>3 modular in parallel in Fig. 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>1 transformer</td>
<td>4 transformers</td>
<td>2 transformers</td>
</tr>
<tr>
<td>RMS current of primary switches</td>
<td>$\pi V_{in}^2/4W_o$</td>
<td>$\pi V_{in}^2/4W_o$</td>
<td>$\pi V_{in}^2/12W_o$</td>
</tr>
<tr>
<td>$I_{ds,SR}$</td>
<td>7.8A</td>
<td>7.8A</td>
<td>2.6A</td>
</tr>
<tr>
<td>RMS current of $L_r$</td>
<td>$\pi V_{in}^2/(2\sqrt{2}, W_o)$</td>
<td>$\pi V_{in}^2/(2\sqrt{2}W_o)$</td>
<td>$\pi V_{in}^2/6\sqrt{2} W_o$</td>
</tr>
<tr>
<td>$I_{ds,SR}$</td>
<td>110A</td>
<td>110A</td>
<td>37.8A</td>
</tr>
<tr>
<td>Total conduction loss of primary switches</td>
<td>$\pi^2 R_d^{(OP)} V_o^2/4W_o^2$</td>
<td>$\pi^2 R_d^{(OP)} V_o^2/4W_o^2$</td>
<td>$\pi^2 R_d^{(OP)} V_o^2/12W_o^2$</td>
</tr>
<tr>
<td>$I_{conduction}$</td>
<td>24.3W</td>
<td>24.3W</td>
<td>8.1W</td>
</tr>
<tr>
<td>Total copper loss of $L_r$ and transformer primary</td>
<td>$\pi^2 R_d^{(SR)} I_o^2$</td>
<td>$\pi^2 R_d^{(SR)} I_o^2$</td>
<td>$\pi^2 R_d^{(SR)} I_o^2$</td>
</tr>
<tr>
<td>$I_{Total}$</td>
<td>153.7W (4.1%)</td>
<td>92.9W (2.5%)</td>
<td>29.6W (0.78%)</td>
</tr>
</tbody>
</table>

Since the switching frequency is high to improve the power density for the proposed LDC, GaN HEMTs are used as the primary side switches to reduce the primary switches loss. The comparison of different 650V switches is shown in Table II. The power loss of GaN HEMT: GSS66508, Silicon MOSFETs: IPL65R099C7 and IPL65R070C7 as primary side switches are compared. Thanks to the low $Q_o$ and $R_{ds(on)}$, GaN HEMT could help reduce the power loss by 3W ~ 9W.

### Table II: Comparison of Different 650V Switches

<table>
<thead>
<tr>
<th>GS66508</th>
<th>IPL65R099C7</th>
<th>IPL65R070C7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_o$</td>
<td>5.8mC</td>
<td>45mC</td>
</tr>
<tr>
<td>$R_{ds(on)}$</td>
<td>102m$\Omega$</td>
<td>165m$\Omega$</td>
</tr>
<tr>
<td>Package</td>
<td>GaN</td>
<td>Package</td>
</tr>
<tr>
<td>Driver loss</td>
<td>17.4mW @6V 500kHz</td>
<td>225mW @10V 500kHz</td>
</tr>
<tr>
<td>Conduction loss</td>
<td>918mW</td>
<td>1485mW</td>
</tr>
<tr>
<td>Total (12 switches)</td>
<td>11.22W</td>
<td>20.52W</td>
</tr>
</tbody>
</table>
III. ANALYSIS OF THE SCC CIRCUIT

A. The proposed LDC with SCC technology

As aforementioned analysis, three LLC converters connected in parallel can reduce the power loss. However, impedance mismatch caused by the tolerance of the resonant components in different phases will lead to current sharing problem in multi-phase converters, which degrades the benefits achieved by the parallel techniques. This paper uses a SCC circuit to achieve current sharing among three phases accurately, and the proposed LDC with SCC circuit is shown in Fig. 4. Three SCC circuits are added into each phase to achieve current sharing.

The equivalent resonant capacitor value can be adjusted to achieve current sharing among three LLC dc-dc converters even under large resonant components tolerance.

Fig. 5 shows the SCC circuit in the first phase of the proposed LDC. The capacitor \( C_{a1} \) is connected in parallel with the switches \( S_1 \) and \( S_2 \). If switches \( S_1 \) and \( S_2 \) are turned on, capacitor \( C_{a1} \) is shorted. If switches \( S_1 \) and \( S_2 \) are turned off, capacitor \( C_{a1} \) is in series with capacitor \( C_{r1} \), and the equivalent resonant capacitor \( C_{r,eq} \) is smaller than \( C_{r1} \).

![Fig. 5. SCC circuit in the first phase of the proposed LDC](image)

To reduce the loss of SCC circuit in [32]-[35], the control strategy of SCC circuit shown in Fig. 6 is adopted in this paper. Defining that \( \alpha \) represents delay phase angle of SCC switches with regard to the current crossover point as shown in Fig. 6. Assuming that a sinusoidal current \( i_{SCC1} \) flows through the SCC circuit, the zero-crossing points of current \( i_{SCC1} \) are at angle 0, \( \pi \), \( 2\pi \) etc. For a positive half cycle, the switch SCC1_2 is turned on at angle \( 2n\pi - \alpha \) and turned off at angle \( 2n\pi + \alpha \), switch SCC1_1 is turned on at angle \( (2n+1)\pi - \alpha \) turned off at angle \( (2n+1)\pi + \alpha \). In the actual implementation, the SCC MOSFET is turned off \( \alpha \) degree after zero crossing point of the resonant current. The SCC MOSFET is turned on when the voltage across \( Ca \) reduced to zero. Since the capacitance of \( Ca \) is large in the real application, such as 10nF, the voltage \( V_Ca \) increases slowly, leading to ZVS turn-off for SCC1_1. After \( C_a \) is fully discharged at \( t_4 \), SCC1_1 is turned on and achieved ZVS turn-on when the capacitor voltage drops to zero. Similarly, switch SCC1_2 can also achieve ZVS turn-on and turn-off.

![Fig. 6. The control strategy of SCC circuit in this work](image)

Fig. 4. Circuit configuration of the proposed three-phase LLC converter with SCC circuit for LDC
TAKING THE FIRST PHASE CIRCUIT AS AN EXAMPLE, FROM [31], THE EQUIVALENT CAPACITANCE OF SCC CIRCUIT CAN BE CALCULATED AS

\[ C_{SCC,phase} = \frac{C_{el}}{2 - (2\alpha - \sin 2\alpha) / \pi} \]  

(1)

From Fig. 5 and (1), the equivalent resonant capacitor \( C_{eq} \) is

\[ C_{eq} = \frac{C_{SCC,phase} C_{r1}}{C_{SCC,phase} + C_{r1}} \]  

(2)

Taking SCC circuit into consideration, the voltage gain of the first phase circuit in the proposed LDC becomes

\[ M = \frac{2nV_o}{V_{in}} = \frac{K}{\sqrt{\left(\frac{\omega_o}{\omega_a}\right)^2 - K^2 - 1}^2 + \left(\frac{\pi^2 \omega_o L_{r1}}{\omega_a}\right)^2 \left[\left(\frac{\omega_o}{\omega_a}\right)^2 - 1\right]^2}} \]  

(3)

where \( L_r \) is load resistance of the first phase, \( K = L_{p1}/L_{r1} \), \( \omega_o = 2\pi f_o \), and \( \omega_a = 1/\sqrt{L_{r1} C_{eq}} \). Similarly, the second and third phase have the same voltage gain shown in (3) when the same resonant parameters are selected.

In LLC dc-dc converter, the resonant components parameters are always designed with the assumption that there is no tolerance among multi phases circuits. According to (1) and (2), a large \( \alpha \) has small effect on the resonant parameters of LLC converter. Therefore, in the proposed LDC, delay angles of all three phases SCC switches \( \alpha \) are set to the maximum value \( \alpha_{max} \) at the beginning. If there is tolerance among three phases, SCC circuit will compensate the resonant parameters and make three phase current sharing by adjusting \( \alpha \).

From (3), the load currents of three phases can be shared by adjusting the delay angle \( \alpha \) of switches SCC1_1~SCC3_2 so that three phase circuits have the same voltage gains at the same switching frequency. Therefore, the total input current and load current will be distributed into three phases equally even if the three phase converters have large resonant components tolerance.

B. Loss analysis of SCC circuit

In the SCC circuit, from Fig. 6, the RMS current flowing through SCC switches \( i_{SCC,1,RMS} \) is

\[ i_{SCC,1,RMS} = \sqrt{\frac{2}{\pi} \int_{\alpha-\alpha}^{\alpha} \left(\frac{2I_{Lr,RMS}}{\pi} \sin(t)\right)^2 dt} \]  

\[ = I_{Lr,RMS} \sqrt{\frac{2\alpha \sin 2\alpha}{\pi} - 1} \]  

(4)

The average absolute value of the current flowing through SCC switches \( I_{SCC,1,AVE,ABS} \) is

\[ I_{SCC,1,AVE,ABS} = \frac{\alpha}{\pi} \sqrt{\frac{2I_{Lr,RMS} \sin(t) dt}{\pi}} = -2\sqrt{2} I_{Lr,RMS} \frac{\cos \alpha}{\pi} \]  

(5)

As ZVS turn-on and turn-off are achieved, there is only conduction loss of two SCC switches. The current \( i_{SCC,1} \) flows through one MOSFET and one body diode of MOSFET in the control strategy of [32]-[35], thus the loss of one SCC circuit in [32]-[35] is

\[ P_{loss,SCC in [32]-[35]} = I_{SCC,1,RMS}^2 R_{ds(on)} + I_{SCC,1,AVE,ABS} V_F \]  

\[ = I_{Lr,RMS}^2 \left(\frac{2\alpha}{\pi} \sin 2\alpha - 1\right)^2 R_{ds(on)} + \frac{2\sqrt{2} I_{Lr,RMS} V_F \cos \alpha}{\pi} \]  

(6)

From Fig. 5 and Fig. 6, current \( i_{SCC,1} \) flows through two MOSFETs in this work, thus the loss of one SCC circuit in the proposed LDC is

\[ P_{loss,SCC in this work} = 2R_{ds(on)} I_{SCC,1,RMS}^2 \]  

\[ = 2 I_{Lr,RMS}^2 \left(\frac{2\alpha}{\pi} \sin 2\alpha - 1\right)^2 R_{ds(on)} \]  

(7)

According to (6) and (7), the loss of one SCC circuit against delay angle \( \alpha \) with different resonant current \( I_{Lr,RMS} \) in [32]-[35] and in this work is shown in Fig. 7. As three SCC circuits are used in the proposed LDC, if \( I_{Lr,RMS} = 4A \) and \( \alpha = 160^\circ \), the total loss of three SCC switches is 11.1W in [32]-[35], while the total loss of three SCC switches is only 1.9W in this work, which can help reduce the power loss by 9.2W.

IV. PARAMETERS DESIGN OF THE LDC

Since the three phase LLC dc-dc converters have the same parameters design in the proposed LDC, only taking the first phase circuit analysis as an example. To ensure the converter operates in the ZVS region of primary switches and ZCS region of the SR, the resonant point (unity voltage gain) is selected based on the maximum input voltage and the minimum output voltage. The transformer turns ratio is determined by

\[ n = N_p : N_s = V_{in,max} : V_{out} \]  

(8)

where, \( N_p \) is the primary turns number and \( N_s \) is the secondary turns number.

With 430V maximum input and 9V minimum output voltage, each transformer turns ratio should be 430V / 9V / 2 = 23.8. However, as 9V is an odd point with less current requirement, the turns ratio is selected as 22:1:1 for each transformer.

For EVs, the maximum output power of the LDC is limited by the voltages across high voltage battery. In this case, load capacity is different at different input and output conditions. Each phase of the LLC dc-dc converter considers maximum 90A

\[ I_{Lr,RMS} = 6A \]  

\[ I_{Lr,RMS} = 4A \]  

\[ I_{Lr,RMS} = 2A \]  

Fig. 7. Loss comparison of the SCC circuit
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\[ M = \frac{nV_o}{V_{in}} = \frac{16 \times 44}{250} = 2.82, \]  

(9)

in this case, quality factor \( Q \) satisfies

\[ Q = \frac{\pi^2 I_o / 3}{8n^2V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times (90 \times 0.6 \times 14 + 16)}{8 \times 44^2 \times 16} \sqrt{\frac{L_{r1}}{C_{r1}}} \]

\[ = 1.882 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \]

When the input voltage is 330V, full load needs to be carried, and the resonant parameters should be designed for this condition. When the output voltage is 16V, the maximum step-up voltage gain is

Case 2:

\[ M = \frac{nV_o}{V_{in}} = \frac{16 \times 44}{330} = 2.13, \]  

(11)

and quality factor \( Q \) satisfies

\[ Q = \frac{\pi^2 I_o / 3}{8n^2V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times (90 \times 14 + 16)}{8 \times 44^2 \times 16} \sqrt{\frac{L_{r1}}{C_{r1}}} \]

\[ = 3.136 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \]

As large \( Q \) value would decrease voltage gain, 14V output 90A load current should also be considered in this design. When the output voltage is 14V, the maximum step-up voltage gain is

Case 3:

\[ M = \frac{nV_o}{V_{in}} = \frac{14 \times 44}{330} = 1.87, \]  

(13)

and quality factor \( Q \) satisfies

\[ Q = \frac{\pi^2 I_o / 3}{8n^2V_o} \sqrt{\frac{L_{r1}}{C_{r1}}} = \frac{\pi^2 \times 90}{8 \times 44^2 \times 14} \sqrt{\frac{L_{r1}}{C_{r1}}} \]

\[ = 4.097 \times 10^{-3} \sqrt{\frac{L_{r1}}{C_{r1}}}. \]

Compared with 100kHz–200kHz resonant frequency in traditional LDC, the resonant frequency between \( L_{r1} \) and \( C_{r1} \) is selected to be around 500kHz to reduce the volume of magnetic components and improve the power-density in this work. According to [38], three sets of resonant parameters are selected to meet the parameters design for the proposed LDC, and the accurate voltage gain curves are given in Fig. 8 by using time-domain analysis method.

As shown in Fig. 8(a), when \( K=3, f_r=546kHz, Q=0.45 \), that is \( L_{r1}=32\mu H, L_p=96\mu H \) and \( C_{r1}=2.7nF \), the maximum voltage gains of the three cases are achievable, and the minimum switching frequency is 0.58\( f_r \). However, the inductance of \( L_p \) is too small, which is difficult to optimize the fringing loss and core loss. As shown in Fig. 8(b), when \( K=5, f_r=546kHz, Q=0.35 \), that is \( L_{r1}=25\mu H, L_p=125\mu H \) and \( C_{r1}=3.4nF \), the maximum voltage gains of the three cases are also achievable, and the minimum switching frequency is 0.47\( f_r \). As shown in Fig. 8(c), when \( K=8, f_r=546kHz, Q=0.25 \), that is \( L_{r1}=18\mu H, L_p=142\mu H \) and \( C_{r1}=4.8nF \), the maximum voltage gains of the three cases can also be achieved, and the minimum switching frequency is smaller than 0.4\( f_r \).
parameters, the second set of resonant parameters $L_r=25\mu H$, $L_p=125\mu H$, $C_r=3.4nF$ are selected, and the resonant parameters of the second and third phase are the same as that of the first phase.

V. MAGNETIC COMPONENTS AND PCB DESIGN OF THE PROPOSED LDC

A. Design of magnetic components

In this work, the center-tap transformer is used with 22:1:1 turns ratio. As shown in Fig. 4, two transformers primary are in series, if $L_{p1}$ is selected as $125\mu H$, $62.5\mu H$ magnetizing inductor is needed in each transformer. As at least 22 turns are designed for transformer primary winding, thus a large air gap is required for the transformers, which means large fringing loss. In the proposed LDC, an external inductor $L_{p1}$ is used so that no air gap is needed for the transformer to improve the efficiency.

If the proposed LDC operates at resonant frequency with 380V input and 14V/270A output, the RMS current flowing through one of the transformer secondary side winding is

$$i_{T_{s},RMS} = \sqrt{2} i_{T_{s,RMS}} = 35.3A,$$  \hspace{1cm} (15)

the RMS current of transformer primary winding is

$$i_{T_{p},RMS} = \frac{\sqrt{2} i_{T_{s,RMS}}}{n} = 2.3A,$$ \hspace{1cm} (16)

and the RMS current $i_{L_{p1}}$ is

$$i_{L_{p1},RMS} = \frac{2\pi V_{T} L_{o}}{4L_{p1}} \times \frac{1}{\sqrt{3}} = 1.3A,$$ \hspace{1cm} (17)

As the converter operates at a switching frequency higher than 260kHz, Litz wire is used to implement the magnetic components to reduce the AC losses caused by skin effect and proximity effect.

According to the current stress shown in (15) - (18), the different litz wires are selected for the magnetic components. The core size, material and structure of all the magnetic components are shown in Table III.

<table>
<thead>
<tr>
<th>Inductor $L_{o1}$</th>
<th>Inductor $L_{o2}$</th>
<th>Transformer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Size</td>
<td>Core Size</td>
<td>Core Size</td>
</tr>
<tr>
<td>PQ32/20</td>
<td>PQ35/35</td>
<td>PQ35/35</td>
</tr>
<tr>
<td>Material</td>
<td>Material</td>
<td>Material</td>
</tr>
<tr>
<td>3C97</td>
<td>3C97</td>
<td>3C97</td>
</tr>
<tr>
<td>Litz Wire</td>
<td>Litz Wire</td>
<td>Litz Wire</td>
</tr>
<tr>
<td>NELC650/44SN</td>
<td>NELC1100/48SN</td>
<td>Copper foil</td>
</tr>
<tr>
<td>Litz Wire/Litz Wire</td>
<td>Litz Wire/Copper foil</td>
<td>three-layer laminated</td>
</tr>
<tr>
<td>Turns</td>
<td>Turns</td>
<td>Turns</td>
</tr>
<tr>
<td>15</td>
<td>44</td>
<td>22:1:1</td>
</tr>
<tr>
<td>Laminated layers</td>
<td>Laminated layers</td>
<td>Laminated layers</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>2 (Primary) / 3 (Secondary)</td>
</tr>
<tr>
<td>Air gap</td>
<td>Air gap</td>
<td>Air gap</td>
</tr>
<tr>
<td>1.5mm</td>
<td>5mm</td>
<td>0mm</td>
</tr>
</tbody>
</table>

Fig. 9 shows the photo of the primary side and secondary side of the transformer. The primary winding uses 22 turns of 2 layers of litz wire. On the secondary side, each of the center-tapped windings is created using 1 turn of three paralleled 20mm × 0.25mm copper foils.

B. Design of PCB board

For the LDC prototype, if only one PCB board is used, magnetic components, controller circuit and active devices should be placed on the same one board. Thus, the vertical space of the structure is not efficiently used because the height of magnetic components is much larger than controller circuit and active devices. The space above the active devices and controller circuit is basically not utilized, which reduces the power density of the converter.

![Fig. 9. Photo of the transformer](image)

![Fig. 10. 3D Model of the proposed LDC](image)
VI. EXPERIMENTAL RESULTS

To verify the analysis, a 3.8kW LDC prototype is built and tested. The series resonant inductor is 25μH, the parallel inductor is 125μH, the resonant capacitor is 3.4nF, the SCC capacitor is 14nF and the transformer turns ratio is \( n_p/n_s = 1:22:1 \). The specifications and parameters of the proposed LDC are given in Table IV.

<table>
<thead>
<tr>
<th>TABLE IV: SPECIFICATIONS AND PARAMETERS OF THE PROPOSED LDC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input voltage</strong></td>
</tr>
<tr>
<td><strong>Output voltage</strong></td>
</tr>
<tr>
<td><strong>Maximum output current</strong></td>
</tr>
<tr>
<td><strong>Maximum output power</strong></td>
</tr>
<tr>
<td><strong>Transformer</strong></td>
</tr>
<tr>
<td><strong>Parallel inductor</strong></td>
</tr>
<tr>
<td><strong>Series inductor</strong></td>
</tr>
<tr>
<td><strong>Series capacitor</strong></td>
</tr>
<tr>
<td><strong>SCC capacitor</strong></td>
</tr>
<tr>
<td><strong>Primary switches</strong></td>
</tr>
<tr>
<td><strong>Secondary switches</strong></td>
</tr>
<tr>
<td><strong>SCC switches</strong></td>
</tr>
<tr>
<td><strong>Input capacitor</strong></td>
</tr>
<tr>
<td><strong>Output capacitor</strong></td>
</tr>
<tr>
<td><strong>Micro-controller</strong></td>
</tr>
</tbody>
</table>

Fig. 11 and 12 show the prototype of the proposed LDC and the test bench. The prototype with 3kW/L power-density and 1.5kg weight is achieved. In the proposed LDC, three interleaved LLC converters are paralleled for reducing the current stress to improve the efficiency, and the SCC circuit is used to make sure three phase current sharing. The liquid cooling is used for heat dissipation of the devices on the main board, and the fan cooling is used for heat dissipation of the magnetic components. Three 90A electronics load is paralleled to provide 270A load. In practice, the highest current tested is 260A due to the power limitation of the electronic load.

As shown in Fig. 13, a wide voltage range 250V~430V input and 9V~16V output is achieved. In Fig. 13(a), input and output voltages are 430V and 14V with 5A load current, and the switching frequency is 324kHz. In Fig. 13 (b), input and output voltages are 250V and 16V with 40A load current, and the switching frequency is 260kHz. In Fig. 13(c), input and output voltages are 330V and 9V with 70A load current, and the switching frequency is 346kHz. From Fig. 13, ZVS turn-on can be achieved in light and heavy load at a wide switching frequency range.

As shown in Fig. 14, input and output voltage are 380V and 14V when the load of the second phase circuit is 90A, delay angle \( \alpha \) is 149°. From Fig. 14, ZVS turn-on and ZVS turn-off can be achieved, and the voltage stress of the switches in SCC circuit is low (around 25V), which verifies the analysis.
Fig. 14. Waveform of the second phase SCC circuit at 380V input and 14V/90A output

(a) SCC capacitor voltage $v_{Ca2}$ and $v_{Ca3}$

(b) the resonant current $i_{Lr2}$ and $i_{Lr3}$

Fig. 15. Waveforms of two-phase circuits operation at 250V input, 14V/100A output

(a) SCC capacitor voltage $v_{Ca2}$ and $v_{Ca3}$

(b) the resonant current $i_{Lr2}$ and $i_{Lr3}$

Fig. 16. Waveforms of three-phase circuits operation at 380V input, 14V/200A output

(a) SCC capacitor voltage $v_{Ca1}$, $v_{Ca2}$ and $v_{Ca3}$

(b) the resonant current $i_{Lr1}$, $i_{Lr2}$ and $i_{Lr3}$

Fig. 17. Waveforms of three-phase circuits operation at 380V input, 14V/260A output

(a) SCC capacitor voltage $v_{Ca1}$, $v_{Ca2}$ and $v_{Ca3}$

(b) the resonant current $i_{Lr1}$, $i_{Lr2}$ and $i_{Lr3}$

Fig. 15 shows the waveforms of the SCC current sharing technology is used in the proposed LDC. When the second and third phase circuits operate at 250V input and 14V output voltage with 100A load current, switching frequency is 269kHz and the delay angles $\alpha$ are 148° and 135° respectively in the second and third phase SCC circuits. Two resonant currents $i_{Lr2}$ and $i_{Lr3}$ are very closely balanced by adjusting the delay angle $\alpha$ in the two SCC circuits.

As shown in Fig. 16, when the three-phase circuits of the proposed LDC operate at 380V input and 14V output voltage with 200A load current, switching frequency is 311kHz and the delay angles $\alpha$ are 144°, 150° and 132° respectively in the three SCC circuits. Fig. 17 shows the waveforms when input is 380V and output is 14V / 260A with three-phase operation. The switching frequency is 305kHz and the delay angles $\alpha$ are 136°, 154° and 126° respectively in the three SCC circuits. From Fig. 16 and 17, the resonant currents of the three phase LLC dc-dc converters are balanced well by adjusting the delay angle $\alpha$ under different operation conditions.
Fig. 18 shows RMS resonant current at 380V input and 14V output with three-phase circuits operation. When load current increases from 140A to 260A, the current sharing error $\sigma_{\text{resonant}}$ is always smaller than 2.5%, which means three phase load currents are very balanced.

Power loss breakdown is given in Fig. 19. In this paper, the optimal SR conduction time is not concerned as there are many methods to optimize the SR conduction time [10], [39]. In the proposed LDC, NCP4305 synchronous rectifier chip is used and constant conduction time 0.825us of SR switches is adopted. If SR conduction time is optimized, the body diode loss of $S_1$-$S_{12}$ could be removed, and the efficiency can be improved further.

Fig. 20 shows the efficiency of single phase, two phase and three phase circuits at 380V input and 14V output. Phase shedding is used to achieve the highest efficiency for each load range. When the input voltage is 380V, single phase circuit operates at from 0A load current to 80A load current, two phase circuits operate from 80A load current to 130A load current and three phase circuits operate from 130A load current to 260A load current.

Fig. 21 shows the efficiency curves of the proposed LDC at different input voltage and 14V output voltage. 95% and higher efficiency can be achieved over the wide load ranges (from 20A load to full load). When the input voltage is 380V and output voltage is 14V, 95.8% efficiency is achieved at 260A load current, and peak efficiency is 96.7%.

Fig. 22 shows the thermal images at 380V input, 14V/260A output with 25°C fluid liquid cooling and fan cooling. The performance of EV LDC as presented in recent literatures [1]-[8], [14]-[17], [45]-[46] and the products [40]-[44] is summarized in Table V for a comprehensive comparison. It shows that with SCC technology, the LDC designed in this paper achieves high efficiency and high power-density at the same time.
TABLE V: COMPARISON BETWEEN THE PROPOSED LDC AND OTHERS LDC

<table>
<thead>
<tr>
<th>Reference</th>
<th>Specification of the Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Topology</td>
</tr>
<tr>
<td>[1]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[2]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[3]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[4]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[5]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[6]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>[7]</td>
<td>Three-level phase-shift half bridge converter</td>
</tr>
<tr>
<td>[8]</td>
<td>Two-stage converters</td>
</tr>
<tr>
<td>[14]</td>
<td>LLC converter</td>
</tr>
<tr>
<td>[15]</td>
<td>LLC converter</td>
</tr>
<tr>
<td>[16]</td>
<td>LLC converter</td>
</tr>
<tr>
<td>[17]</td>
<td>LLC converter</td>
</tr>
<tr>
<td>[40]</td>
<td>-</td>
</tr>
<tr>
<td>[41]</td>
<td>-</td>
</tr>
<tr>
<td>[42]</td>
<td>Buck-Boost converter + Series resonant converter</td>
</tr>
<tr>
<td>[43]</td>
<td>-</td>
</tr>
<tr>
<td>[44]</td>
<td>-</td>
</tr>
<tr>
<td>[45]</td>
<td>Buck converter + LLC DCX</td>
</tr>
<tr>
<td>[46]</td>
<td>Phase-shift full bridge converter</td>
</tr>
<tr>
<td>The proposed LDC</td>
<td>SCC-LLC converter</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

To reduce the conduction loss at high load current, three phase interleaved LLC dc-de converters in parallel are designed for EV LDC in this paper. SCC circuit is added into resonant tank to achieve current sharing among three phases. In the proposed LDC, GaN HEMTs are used in transformer primary side, allowing the switching frequency to be increased while the volume of the circuit is reduced. ZVS turn-on of the primary switches and ZCS turn-off of secondary SRs are achieved. ZVS operation and low conduction loss of the SCC circuit switches are also achieved. By adjusting the delay angle $\alpha$ of SCC, three phase resonant currents are balanced. Two PCB board structure and the liquid cooling cold plate are designed to improve the power-density and limit the temperature rise. The proposed LDC achieves an efficiency of 95.8% at 260A load current and a peak efficiency of 96.7% with a 3kW/L power-density. Phase shedding is used for different load currents, which results in high efficiency over the full load range. Compare with others LDC, the proposed LDC achieves both high efficiency and high power-density simultaneously.

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IEEE POWER ELECTRONICS REGULAR PAPER/LETTER/CORRESPONDENCE


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IEEE POWER ELECTRONICS REGULAR PAPER/LETTER/CORRESPONDENCE


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