

A Modified Equivalent Circuit Based Electro-Thermal Model for Integrated POL Power Modules

Wenbo Liu, Sam Webb, Yan-Fei Liu, *Fellow,*
IEEE

Department of Electrical and Computer Engineering
Queen's University,
Kingston, Canada
liu.wenbo@queensu.ca, yanfei.liu@queensu.ca

Laili Wang and Doug Malcolm

Sumida Technologies Inc.
Sumida Corporation
Kingston, Canada
laili_wang@us.sumida.com

Abstract— this paper presents an improved thermal equivalent circuit model which provides an accurate thermal and loss estimation for integrated power modules. Thermal analysis is a critical issue for power electronic systems, it estimates the thermal performance of power devices and enables a flexible converter design. Unlike the conventional thermal models, the modified analytical thermal model takes the temperature dependency of loss into account and achieves a more realistic electro-thermal prediction. The thermal and loss analysis is the interaction of temperature and loss thus its accuracy is significantly improved. Finite element analysis (FEA) and experiment were performed to validate the modified thermal equivalent circuit model and the estimation shows a good agreement with the verifications.

Keywords – power converters, thermal modeling, temperature dependency, FEA simulation

I. INTRODUCTION

During recent decades, the power density of power electronic devices keeps increasing steadily due to the requirement of smaller size. The requirement of quick and accurate thermal analysis draws more attention as a consequence [1]-[3]. Integrated point-of-load (POL) power modules shown in Fig. 1 are one of the products in great need of thermal analysis due to their high power density, small size and usually hot environment. Buck converters shown in Fig. 2 is a major type of point of load converters and has taken a large portion of the integrated power module market. They are widely used as power supplies in computer, telecommunication and other portable devices. For capsulated point-of-load converters with 5-20A full load current, the power density can achieve $500\text{W}/\text{in}^3$, and for the converters with less than 5A load current the maximum power density can exceed $1000\text{W}/\text{in}^3$. Thermal modeling of integrated power solutions is critical for system design and optimization. An accurate thermal estimation can provide a reasonable reference for the selection of current rating and switching frequency to achieve better performance and avoid system failure. It can also provide parameters including thermal resistance and derating curves which are always required in the datasheet [4]-[6].

Thermal equivalent circuit models, which utilizes fundamental circuit components to simulate thermal performance are a fast and effective way for thermal

modeling. Several emerging modeling methods make use of advanced simulation software and mechanical disassembling technologies to achieve more detailed and convincing thermal models [1][2]. For steady-state, the capacitors are fully charged so that they could be ignored and the two-resistor compact model shown in Fig. 3 is obtained. This model can be applied to the ICs or power modules to estimate their thermal performance. The junction to case thermal resistance (θ_{JC}) and junction to ambient resistance (θ_{JA}) are critical parameters that enable the estimation of junction temperature [7]. The thermal resistance values can be found in the datasheet and the junction temperature can be simply calculated as long as the heat dissipation is obtained. Methods such as thermal simulation and temperature sensing are utilized in addition to modelling to assist in thermal analysis [8]-[10].

However, several factors limits the accuracy of the thermal equivalent circuit models. For the actual integrated point of load converters, both semiconductor loss and inductor loss are affected by the temperature which is not

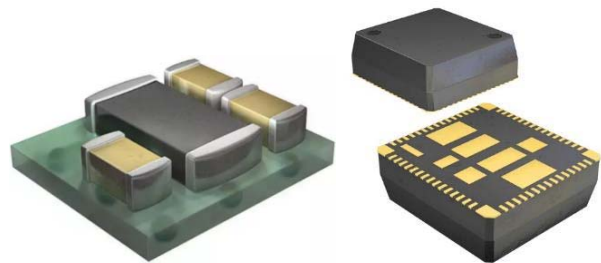


Fig. 1. Encapsulated Power Modules

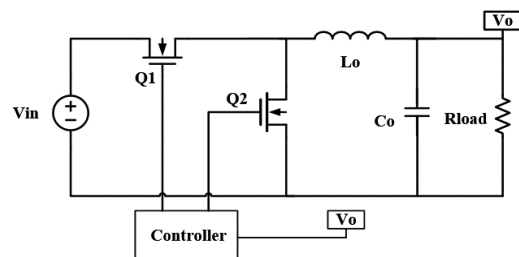


Fig. 2. Step-down Buck Converter Circuit

considered as an input in the conventional thermal models. As a majority-only carrier, the turn-on resistance of MOSFET increases as the temperature rises. Also the resistivity of copper is in proportion to temperature rise so that more winding loss will be generated when the temperature gets higher. Moreover, higher loss in turn results in a further temperature rise [11]-[15]. On the other hand, temperature rise also changes the ability of heat dissipation which also affects the thermal performance. Therefore, the actual loss is more or less different from calculation depending on the operating condition and it can result in a serious error to the prediction of thermal model. In consequence, adding the interaction of temperature, loss and heat transfer coefficient into the model is necessary for thermal analysis. Meanwhile, thermal resistances defined in two-resistor compact models only apply to normal ICs which are in compact package with only one heat source, or the small packages where the temperature is almost evenly distributed on the surfaces. For the power modules or integrated multi-phase converters with more than one source of heat, each heat source has an impact on the others and the distribution of heat dissipation is not uniform. Thus more nodes and resistors need to be added into the circuit model.

In this paper, a modified thermal equivalent circuit model which includes temperature dependency of loss into account and achieves a more accurate thermal estimation. The circuit topology is also modified to provide the details of multiple heat sources. The paper is organized as follows: Section II analyzes loss of the target converter, equations of the losses are derived and assigned in the corresponding part of power module. Section III constructs a modified circuit topology based on Foster model with increased reliability. Section IV integrates the information in Section II and III to accommodate the circuit model and predict the thermal performance. Section V performs a series of simulations and makes a comparison between circuit model, finite element analysis (FEA) model and experimental result. Extending research including the impact of temperature on different facts are also presented in this section. Section VI concludes the paper.

II. LOSS ANALYSIS WITH TEMPERATURE DEPENDENCY

This section introduces the method approaching loss breakdown of the target power converter which is a crucial input of the equivalent thermal model. The heat sources in this case are consist of: regulator loss including switching loss, conduction loss, gate driver loss and quiescent loss; inductor loss including winding loss and core loss. The study case in this paper is a non-isolated DC-DC Buck converter with the input and output specifications shown in Table I. R_{ds_on} of high side switch is 20mΩ and it is 10mΩ for the low side. Fig. 4 shows the isometric drawing of the integrated point of load converter, it consists of a voltage regulator

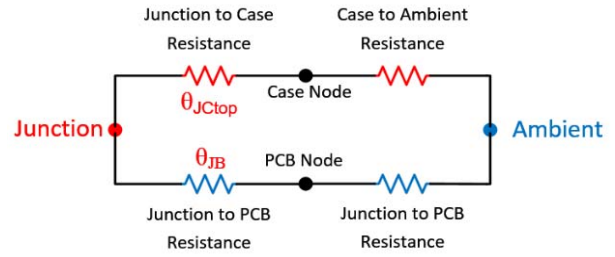


Fig. 3. Two-Resistor Compact Model

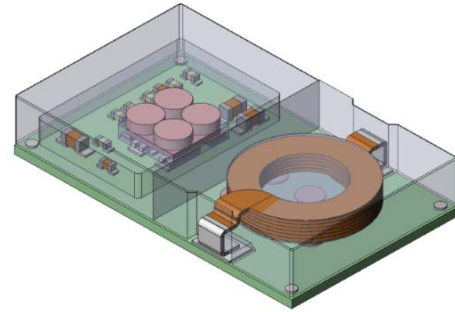


Fig. 4. Isometric Drawing of the Integrated Power Module

(integrates two switches and a controller, left side) and an inductor (right side) [7]. The regulator IC locates in a cavity and the inductor core serves as the case of power module. The total loss of the POL converter can be separated into two categories: the temperature dependent part and the temperature independent part. Each part is estimated and serves as a heat source in the thermal model [16]-[21].

A. Temperature dependent part: winding loss, conduction loss and core loss

The increasing of winding loss and semiconductor switching loss together are the most significantly parameters affected by temperature. The winding loss which is consist of DC winding loss and AC winding loss is determined by (1)-(2):

$$P_{winding} = (P_{t0_dc} + P_{t0_ac})(1 + \alpha(T - 25^{\circ}\text{C})) \quad (1)$$

$$P_{t0_ac} = I_{pk_rms}^2 R_{ac} \quad (2)$$

Where P_{t0_dc} is the DC winding loss calculated by I^2R under room temperature and P_{t0_ac} is the AC loss under same condition. I_{pk_rms} is the rms value of current ripple and R_{ac} is the AC winding resistance which is measured with frequency swing by LCR meter. T is the operating temperature and α is the thermal coefficient of copper, which is 0.00386. Basically DC loss dominates the total winding loss so small direct current resistance (DCR) is always a critical design objective [22].

TABLE I. PARAMETERS OF THE STUDIED INTEGRATED POL CONVERTER

Input voltage V_{in}	Output voltage V_{out}	Maximum output current I_{out}	Switching frequency f_{sw}	High switch on- resistance $R_{ds_on_hs}$	Low switch on- resistance $R_{ds_on_ls}$	Dimensions (mm)
12V	5V	8A	780kHz	20mΩ	10mΩ	15*9*2.8

Conduction loss of switches considering temperature is the most critical part of loss analysis. The R_{ds_on} -temperature curve is always not available, therefore experimental method is applied to obtain the increased conduction loss function of temperature. Due to that switching loss and quiescent loss are independent on temperature, the increased regulator loss is the same as increased conduction loss. Table II presents the measured losses and junction temperature at different load current (temperature is measured by IR camera). The initial losses are measured at the moment of startup, ΔP_{cond} is the ratio of increased conduction loss which is the difference of steady-state loss and initial IC total loss divided by calculated conduction loss. The initial conduction loss at room temperature is (3):

$$P_{cond_0} = \frac{D}{3}(I_{max}^2 + I_{max}I_{min} + I_{min}^2)R_{ds_on_hs} + \frac{1-D}{3}(I_{max}^2 + I_{max}I_{min} + I_{min}^2)R_{ds_on_ls} \quad (3)$$

Where D is the duty ratio of the target Buck converter, the resistances are exactly the values from the datasheet. With the curve fitting method applied to the measured temperature and loss, a linear function of temperature controlled conduction loss is obtained (4):

$$P_{cond} = P_{cond_0}(1 + \Delta P_{cond}\%) \quad (4)$$

And Fig. 5 illustrates this curve fitting plot.

Core loss is another temperature dependent factor in the model. To complete the model, core loss value is simulated in Maxwell FEA software with a pre-estimated operating temperature and is manually assigned into the thermal model. Core loss of ferrite core is determined by the curve fit loss equation (5):

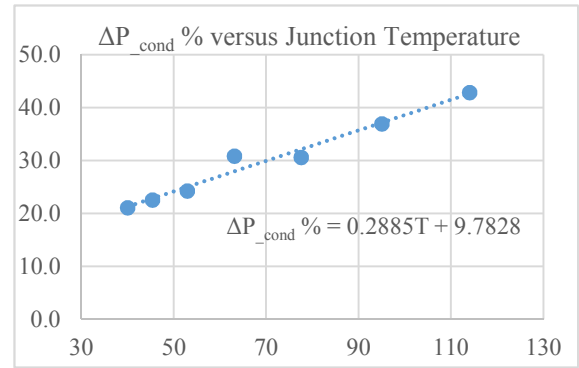


Fig. 5. Linear Fitted Curve: $\Delta P_{cond}\% = f(T)$

$$P_{core} = aB_{pk}^b f^c \quad (5)$$

Where a , b and c are the curve fitted coefficients obtained from the core sample test. Core loss is not affected by temperature according to (3), however, for different operating temperatures, the B-H curve is revised to correspond the actual flux density swing and the core loss values are obtained.

B. Temperature independent loss: switching loss, gate drive loss, etc.

Switching loss of the power converters is not affected by temperature because the gate capacitance is unaffected by temperature [3]. The switching charge Q_{sw} and switching speed keep unchanged, so the loss remains the same. The high side switching loss P_{sw} and gate drive loss P_{gate} are calculated by (6)-(7):

$$P_{sw} = V_{in} \cdot I_{out} \cdot f_{sw} \cdot \frac{Q_{sw}}{I_g} \quad (6)$$

$$P_{gate} = Q_g \cdot V_{drive} \cdot f_{sw} \quad (7)$$

Where I_g is the gate current and V_{drive} is the gate driver voltage. Besides the losses, thermal resistances are required to building a thermal equivalent circuit. FEA simulation is applied here to obtain the conduction thermal resistance. Moreover, convectional thermal resistance which integrates means of convection and radiation to dissipate heat from the module to the ambient is affected by the heat transfer coefficient. Thus its value is dependent on the ambient temperature. It is also simulated in ANSYS FEA software and then is assigned in the model.

III. MODIFICATION ON EQUIVALENT CIRCUIT TOPOLOGY

This section presents the concept of the modification on the equivalent circuit model. According to the isometric drawing shown in Fig. 4, the size of the power module is 15mm*9mm, which is much larger than the voltage regulator itself. With two different amount of power losses in IC and inductor, the temperature will not distribute uniformly. The concept of the proposed thermal resistance model is illustrated in Fig. 6, the inductor winding is modelled as the second heat source and two more paths of heat transfer are added into the model. In order to describe the junction temperature more precisely, two direct case nodes (IC top

TABLE II. MEASURED LOSSES AND TEMPERATURE

Load current (A)	2	3	4	5	6	7	8
Initial regulator loss (W)	0.385	0.506	0.739	1.030	1.435	1.886	2.49
Steady-state regulator loss (W)	0.401	0.538	0.799	1.145	1.597	2.150	2.89
Calculated conduction loss (W)	0.074	0.145	0.245	0.373	0.529	0.713	0.93
IC temperature (°C)	40	45.4	52.9	63.1	77.6	95	114
ΔP_{cond} (%)	21.1	22.6	24.3	30.8	30.6	37.0	42.9

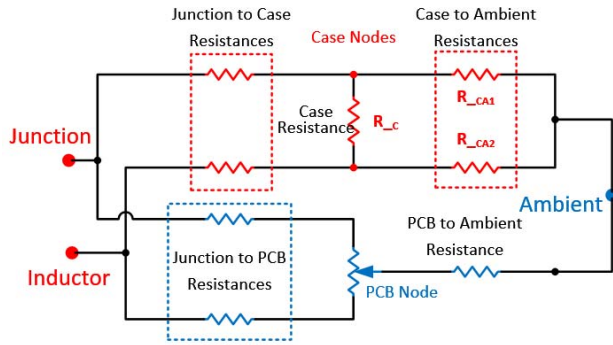


Fig. 6. Modified Thermal Equivalent Circuit Model

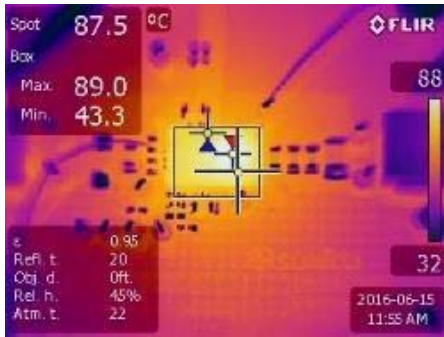


Fig. 7. Thermal Image of the Integrated Converter with 2 Hot Spots

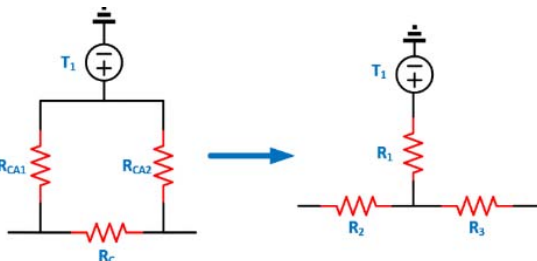


Fig. 8. Δ - Y Transform of Thermal Resistances

case node and inductor top case node) are used to model the junction to case node. The IC top case node is the closest point to the regulator on the case and it reflects the junction temperature directly. These two nodes can provide a more reliable estimation of the IC and inductor winding temperatures. R_{CA1} represents the IC top case node to ambient thermal resistance and R_{CA2} is the inductor case node to ambient thermal resistance. One more thermal

resistance R_c is added between the case nodes because the thermal resistance of the case is not negligible and there is a temperature drop between the nodes.

In addition to the typical power module, the idea of divided heat sources and direct IC top and inductor case nodes can be applied to modeling of multi-phase Buck converters. The equivalent circuit model of a single phase power module is shown in Fig. 6, more case resistances are added into the model. Fig. 7 shows the thermal image of a normal Buck power module [23]-[26].

Generally, the equivalent circuit model uses only one resistor to represent the thermal resistance between the case and ambient, so Δ - Y transform is applied in order to combine R_{CA1} and R_{CA2} into the case to ambient resistor R_1 which still represent for the case to ambient thermal resistance. The equivalent resistances in Fig. 8 are calculated by (8)-(10).

$$R_1 = \frac{R_{CA1}R_{CA2}}{R_{CA1}+R_{CA2}+R_c} \quad (8)$$

$$R_2 = \frac{R_cR_{CA1}}{R_{CA1}+R_{CA2}+R_c} \quad (9)$$

$$R_3 = \frac{R_cR_{CA2}}{R_{CA1}+R_{CA2}+R_c} \quad (10)$$

Benefiting from the added case nodes which correspond the hot spots on the top case of power module, the impact of junction to case and winding to case thermal resistance can be observed. Based on the loss calculation with 22°C ambient temperature, a pre-thermal model is built and the basic thermal performance can be estimated. **Error! Reference source not found.** shows the simulated temperatures of the case nodes sweeping the thermal resistance between the voltage regulator and module top case, which can be realized by changing the potting material inside the power module. Fig. 9 illustrates the temperature curves shown in **Error! Reference source not found.**, it can be observed that the junction temperature reduces significantly with the decrease of junction to case thermal resistance but the case node temperature rises up. This result gives a clear impression on the case temperature. Fig. 10 demonstrates the temperatures of winding and the case node close to it, versus different thermal resistances between the coil and the case. The case temperature is only slightly affected by thermal resistance because the coil is very close to the ambient in the structure of the PSI² technology [18].

TABLE III. COMPARISON OF DIFFERENT 3D CONFIGURATIONS

Variables	The open frame version	Normal glue droplet	Silicone glue droplet	Filled with thermal paste
R4(K/W)	NA	120	60	25
R5(K/W)	16	16	16	15
Junction temperature in analytical model(°C)	NA	107.3	104.9	100.5

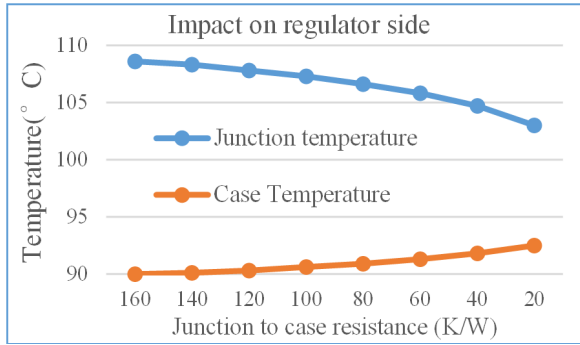


Fig. 9. Temperature versus junction to case resistance

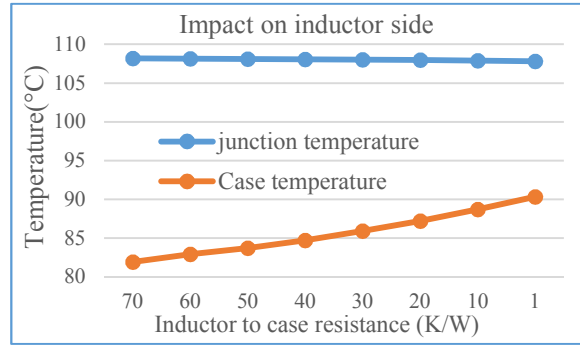


Fig. 10. Temperature versus Inductor to Case Resistance

IV. PRINCIPLE OF THERMAL EQUIVALENT CIRCUIT MODEL

This section presents the modified thermal model based on the integrated power module and its loss analysis discussed in section II. The final thermal model combines the features of modified equivalent circuit and revised temperature dependent loss. The diagram shown in Fig. 11 shows the flow of proposed thermal analysis method: first, fundamental loss breakdown is pre-calculated by the electrical parameters and simulation is performed to obtain thermal resistance values of each part in the power module. Second, the junction and inductor temperature are generated with the variables. If the mathematical method is used to calculate this iteration, for normal heat transfer problems, the temperature distribution is determined by the Fourier's equation, the differential form is (11):

$$\vec{q} = -R\nabla T = -\left(R_x \frac{dT}{dx} + R_y \frac{dT}{dy} + R_z \frac{dT}{dz}\right) \quad (11)$$

Where \vec{q} the vector of heat flow, R is the thermal resistance. For the actual power product, the temperature of each node on the power module can be calculated (12):

$$T_n = \sum_{i=1}^n R_i P_i + T_{ambient} \quad (12)$$

Where R_i and P_i represent for the heat sources and the thermal resistance between the source and nodes. The temperatures provide feedback to the loss model and new loss values are generated, a number of iteration processes are required to obtain a steady-state solution with an acceptable error.

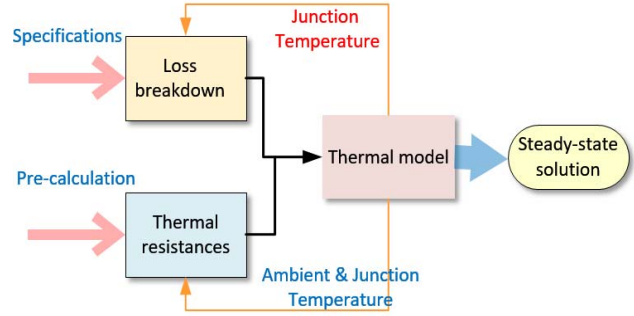


Fig. 11. Temperature versus junction to case resistance

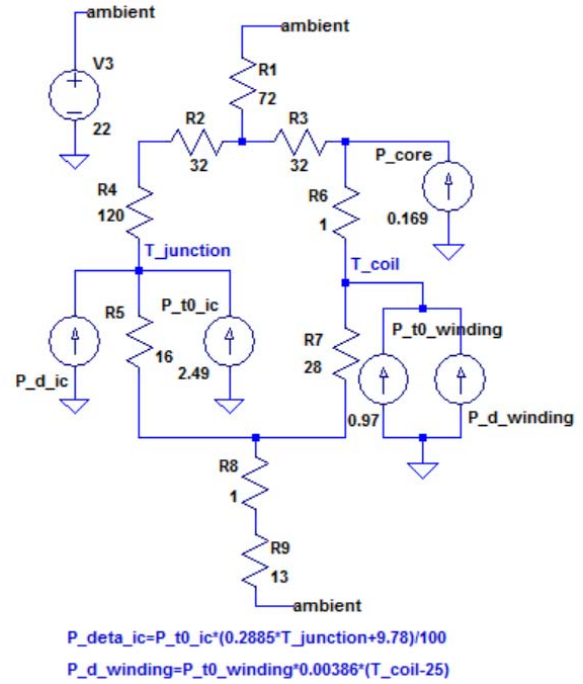


Fig. 12. Proposed Simulation Model (Room Temperature)

Compared with the math model, the circuit model shares the same flow of modeling, but with SPICE simulation software it is much easier and more straightforward. As shown in Fig. 12, the thermal equivalent circuit utilizes voltage controlled current source as the temperature depended heat source. The simulation environment is LTSPICE. The target of modeling is the steady-state solution of a DC-DC converter, so capacitors which represent for the transient thermal capacity are ignored. **Error! Reference source not found.** shows the definition of the thermal resistances and heat sources in the circuit. The value of thermal resistances are simulation with FEA.

Among these values, R1 and R9 are dependent on the temperature because the heat transfer of air increases with the temperature. The surface to ambient thermal resistances consist of convection resistance and radiation resistance, and the radiation thermal resistance from the source to ambient decreases with the temperature. At room temperature, the radiant heat is always less than 30% of convective heat, but

TABLE IV DEFINITION AND VALUES FOR THERMAL MODEL

Designator	Thermal resistance/ Power loss	Value
R ₁	Equivalent convection thermal resistance case to ambient	72K/W
R ₂	Equivalent thermal resistance in the case	32K/W
R ₃	Equivalent thermal resistance in the case	32K/W
R ₄	Contact thermal resistance from the regulator IC to the case	120K/W
R ₅	Joints from the regulator to the substrate	16K/W
R ₆	Thermal resistance between the coil and the magnetic material case	1.2K/W
R ₇	Joints thermal resistance from the pin of the coil through the solder to the substrate	28K/W
R ₈	Joints thermal resistance of the module, from the substrate to the host board	1.5K/W
R ₉	Thermal board convection resistance, from the top of the host thermal board to ambient	13K/W
P _{i0_ic}	First power dissipation by regulator loss	2.49W
P _{core}	Second power dissipation by core loss	0.17W
P _{i0_winding}	Third power dissipation by winding loss	0.97W

as the temperature rises the portion of radiant heat increases. The radiation of heat follows the equations (13)-(14):

$$P_{rad} = \sigma A(T_s^4 - T_a^4) \quad (13)$$

$$R_{radiation} = (T_s - T_a)/P_{rad} \quad (14)$$

Where P_{rad} is the power of radiant heat, σ is a constant, A is the surface area, T_s is the surface temperature, T_a is the ambient temperature. The changing resistances are simulated and put into the model manually. The other thermal resistances present for the resistivity in heat conduction through the solid parts in the module do not significantly impact the temperature.

With all the function of losses are derived and other values confirmed, the model is built as Fig. 12 in LTSPICE and simulation results can be achieved to provide estimated thermal performance. The simulation results by the equivalent circuit model will be discussed in section V.

V. COMPARISON OF SIMULATION AND TEST

The estimation of losses and temperature by the proposed correlation model is shown in Fig. 13. Case node #J represents the hot spot close to the voltage regulator on the top case while case node #L is the spot close to the winding. The maximum temperature of regulator, which is regarded as the junction temperature is 113.3°C and the inductor coil temperature is 95°C. With the purpose of comparison and verification, FEA simulation and experiment were performed. Fig. 14 Fig. 14 shows the FEA simulation with ANSYS and Fig. 15 shows the thermal image taken with IR camera. Both of the results match the thermal model closely and the error is less than 1%. The FEA simulation provides a much more detailed and accurate result than the circuit

model, however it usually takes more than 90 minutes to complete a task. Using the two methods together is an ideal method to analyze thermal performance.

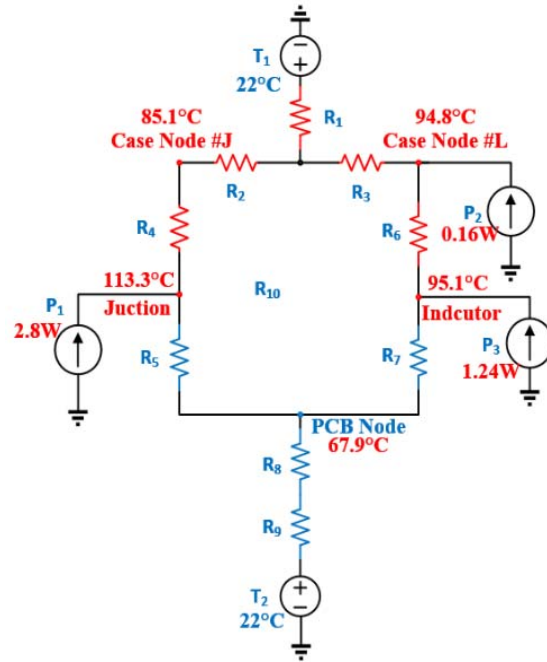


Fig. 13. Thermal Estimation by the Proposed Model

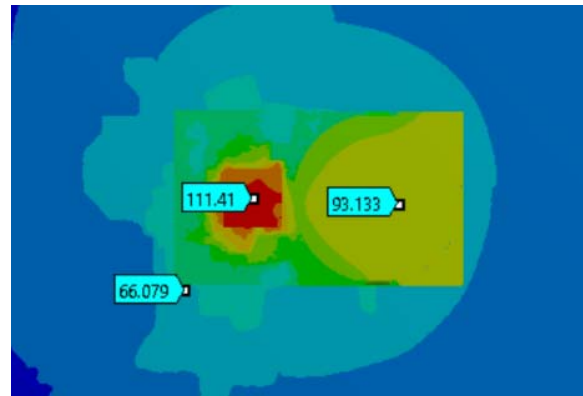


Fig. 14. FEA Simulation with Steady-state Losses



Fig. 15. Steady-state Thermal Image with 8A Load Current

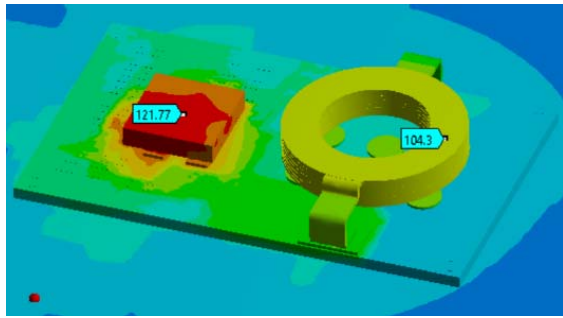


Fig. 16. FEA simulation with Steady-State Loss at 40°C

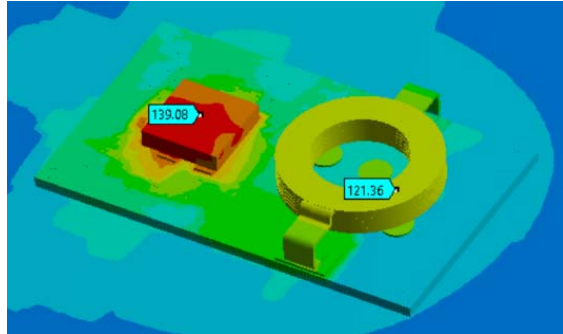


Fig. 17. FEA simulation with Steady-State Loss at 55°C

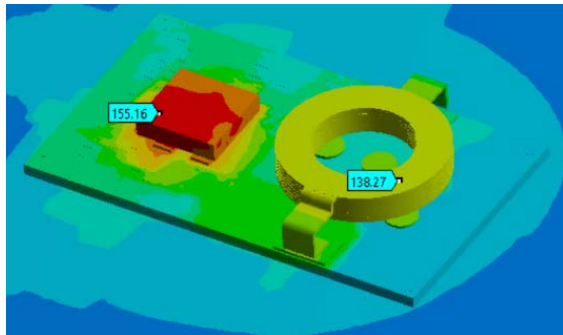


Fig. 18. FEA simulation with Steady-State Loss at 70°C

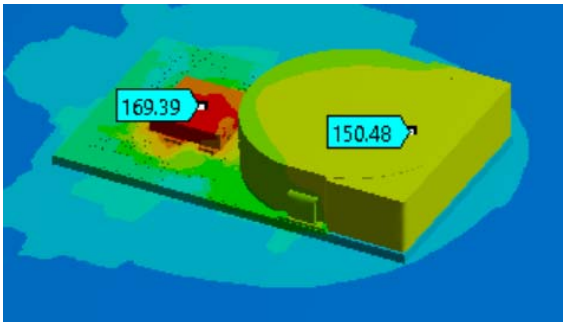


Fig. 19. FEA simulation with Steady-State Loss at 80°C

Fig. 16 to Fig. 19 present the thermal images which show the junction and core temperatures when the ambient temperature varies from 40°C to 80°C. The losses are pre-calculated to fit this condition. According to these images as well as Fig. 14, the temperature rise in 80°C ambient temperature (89.5°C) is a little lower than the rise in 22°C

TABLE V THERMAL PERFORMANCE AND LOSS VERSUS AMBIENT TEMPERATURE

Ambient temperature (°C)	22	30	40	50	60	70	80
IC Loss (W)	2.89	2.91	2.94	2.96	2.98	3.01	3.03
Temperature rise (°C)	91.3	92.5	93.5	91	90.1	90.4	89.5
Winding Loss (W)	1.23	1.26	1.30	1.33	1.37	1.40	1.44
Temperature rise (°C)	72.8	74.4	75.5	73.5	72.9	73.5	72.9

ambient (91.3°C) although the loss is higher indeed. This phenomenon indicates that the temperature has a large impact on the heat transfer coefficient so that heat dissipation is improved in high ambient temperature so that the temperature rise does not increase with the higher winding and conduction loss.

According to the analysis above, increasing the loss and decreasing the thermal resistance are two methods that temperature rise imposes error into the thermal simulation. In order to study the coupling effect of these two factors, a series of simulation were performed. 0V presents the losses and temperature rises versus different ambient temperature, 8A load current is applied. The losses keep increasing with the operating temperature of power module according to the results and the temperature rise of IC increases between 22°C and 50°C ambient temperature. While the switches operating temperature is higher than around 150°C or the ambient temperature is higher than 50°C, it starts to drop.

Fig. 20 shows the junction and coil temperatures in the circuit model at different ambient temperature and load conditions. Series 1 is the junction temperature at 8A load current, series 2 is the coil temperature at 8A load; series 3 is the junction with 6A output current and series 4 corresponds the coil at 6A load. It can be observed that for the studied case temperature rise is almost in proportion to the ambient at the same load because the variation of thermal resistance cancels the effect of increased loss. However, in some special cases the error could be large enough to affect the

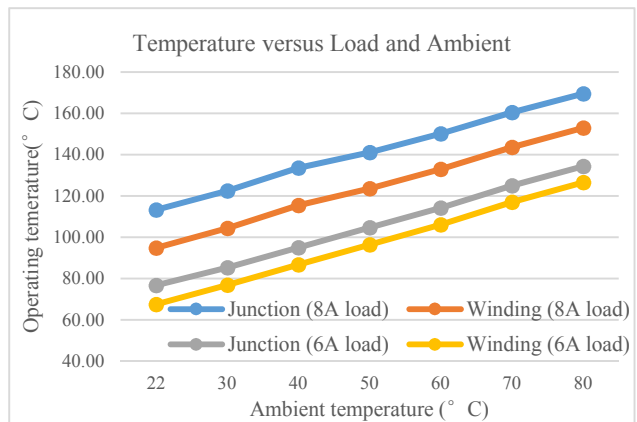


Fig. 20. Thermal Estimation by the Proposed Model

performance of thermal design and the model can be utilized to reduce this error.

VI. CONCLUSION

This paper proposes an improved thermal equivalent circuit model to help analyze the steady-state loss and thermal performance at different ambient and load conditions. The temperature dependency of loss is taken into account and a correlation circuit model which uses voltage controlled current source to simulate the variable electrical loss is built. A number of simulations are performed to verify the model and analyze the effect of temperature dependency. It is noted that temperature affects two factors of the thermal model. One is the increased loss, the other is the decreased thermal resistance. The proposed thermal model takes these two factors into account and the accuracy and reliability is significantly improved. The impact of temperature on heat transfer coefficient will be quantified and the model will be further modified in the future.

REFERENCES

- [1] Trajin, B., Vidal, P. E., & Viven, J. (2015, September). Electro-thermal model of an integrated buck converter. In *Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015 17th European Conference on (pp. 1-9). IEEE.
- [2] Bahman, A. S., Ma, K., & Blaabjerg, F. (2015, March). A novel 3D thermal impedance model for high power modules considering multi-layer thermal coupling and different heating/cooling conditions. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 1209-1215). IEEE.
- [3] Jonathan Dodge, P.E. Feb 2006, Power MOSFET Tutorial (Application note APT0403). Retrieved from Advanced Power Technology website: <http://www.microsemi.com/>
- [4] Jorge, L. M. M., Jorge, R. M. M., Fujii, F., & Giudici, R. (1999). Evaluation of heat transfer in a catalytic fixed bed reactor at high temperatures. *Brazilian Journal of Chemical Engineering*, 16(4), 407-420.
- [5] Bryant, A., Parker-Allotey, N. A., Hamilton, D., Swan, I., Mawby, P. A., Ueta, T., ... & Hamada, K. (2012). A fast loss and temperature simulation method for power converters, Part I: Electrothermal modeling and validation. *IEEE transactions on power electronics*, 27(1-2), 248-257.
- [6] Swan, I., Bryant, A., Mawby, P. A., Ueta, T., Nishijima, T., & Hamada, K. (2012). A fast loss and temperature simulation method for power converters, part II: 3-D thermal model of power module. *IEEE Transactions on Power Electronics*, 27(1), 258-268.
- [7] JEDEC standard: Jesd 51 "Methodology for the thermal measurement of component packages", JEDEC solid state technology association.
- [8] Martin März, Paul Nance. Thermal modeling of power-electronic systems. Retrieved from Infineon Technology AG website: <http://www.infineon.com/>
- [9] Thomas Schutze. June 2008, Thermal equivalent circuit models (Application note AN2008-03). Retrieved from Infineon Technology AG website: <http://www.infineon.com/>
- [10] Mauney, C. (2006). Thermal considerations for surface mount layouts. In *Texas Instruments Portable Power Supply Design*, Seminar. <http://www.ti.com/>
- [11] Ménager, L., Martin, C., Allard, B., & Bley, V. (2006, November). Industrial and lab-scale power module technologies: A review. In *IEEE Industrial Electronics, IECON 2006-32nd Annual*
- [12] Skoplaki, E., & Palyvos, J. A. (2009). On the temperature dependence of photovoltaic module electrical performance: A review of efficiency/power correlations. *Solar energy*, 83(5), 614-624.
- [13] Takahashi, Tomohiro, and Q. Yu. "Precision evaluation for thermal fatigue life of power module using coupled electrical-thermal-mechanical analysis." *Electronics Packaging Technology Conference (EPTC), 2010 12th IEEE*, 2010:201-205.
- [14] Hirohata, K., Hisano, K., Mukai, M., Aoki, H., Takubo, C., Kawakami, T., & Pecht, M. G. (2010). Coupled thermal-stress analysis for FC-BGA packaging reliability design. *Components and Packaging Technologies, IEEE Transactions on*, 33(2), 347-358.
- [15] Yamada, Y., Yu, Q., Takahashi, T., & Takagi, Y. (2012, December). Study on thermal design due to downsizing of power module using coupled electrical-thermal-mechanical analysis. In *Electronic Materials and Packaging (EMAP), 2012 14th International Conference on* (pp. 1-7). IEEE.
- [16] Wang, L., Malcolm, D., Liu, W., & Liu, Y. F. (2016, March). Thermal analysis of a magnetic packaged power module. In *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE* (pp. 2095-2101). IEEE.
- [17] Wang, L., Malcolm, D., & Liu, Y. F. (2016, March). An innovative power module with power-system-in-inductor structure. In *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE* (pp. 2087-2094). IEEE.
- [18] Cooper, David. "Power Module Integration: A new approach." *IEEE Power Electronics Magazine* 3.3 (2016): 31-36.
- [19] Liu, Tianshu, et al. "A novel asymmetrical three-level BUCK (ATL BUCK) converter for point-of-load (POL) application." *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015.
- [20] Wang, L., Hu, Z., Liu, Y. F., Pei, Y., Yang, X., & Wang, Z. (2013). A Horizontal-Winding Multipermeability LTCC Inductor for a Low-profile Hybrid DC/DC Converter. *Power Electronics, IEEE Transactions on*, 28(9), 4365-4375.
- [21] Wang, L., Hu, Z., Liu, Y. F., Pei, Y., & Yang, X. (2013). Multipermeability Inductors for Increasing the Inductance and Improving the Efficiency of High-Frequency DC/DC Converters. *Power Electronics, IEEE Transactions on*, 28(9), 4402-4413.
- [22] Kolar, J. W., Biela, J., Waffler, S., Friedli, T., & Badstuebner, U. (2010, March). Performance trends and limitations of power electronic systems. In *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on* (pp. 1-20). IEEE.
- [23] Liu, Y. O., & Kinzer, D. (2011, April). Challenges of power electronic packaging and modeling. In *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2011 12th International Conference on* (pp. 1-9). IEEE.
- [24] Hodgkin, A. L., & Katz, B. (1949). The effect of temperature on the electrical activity of the giant axon of the squid. *The Journal of Physiology*, 109(1-2), 240.
- [25] Edmunds, L. (2002). Heat Sink Characteristics. *International Rectifier Application notes* A-1057.
- [26] Numakura, K., Emori, K., Yoshino, Y., Hayami, Y., Hayashi, T., (2016, September). Direct-cooled power module with a thick Cu heat spreader featuring a stress-suppressed structure for EV/HEV inverters. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE.