

# A Systematic Method to Synthesize New Transformerless Full-bridge Grid-tied Inverters

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**Abstract**— many inverter topologies have been proposed to eliminate the leakage current of transformerless Full Bridge Grid-Tied photovoltaic (PV) inverters. These include implementations such as the H5, H6, and HERIC topologies, among others. In this paper, a new full bridge topology synthesis method, called the MN synthesis method, is proposed. The MN method introduces two criteria that can be used to synthesize all of the possible topologies, including the existing topologies as well as new simplified topologies. This method concludes that there only 15 simplified topologies are available. Most simplified topologies from MN method have been verified by existing papers and patents.

## I. INTRODUCTION

In single phase grid-tied systems, the isolation transformer's location is often chosen to achieve a higher system efficiency, while also considering the system size, weight, and resulting cost due to spatial requirements... However, the resulting configuration can cause the common-mode (CM) ground leakage current to appear on the parasitic capacitor between the PV panels and the ground [1]-[3]. The CM current path for grid-tied transformer-less PV inverter systems is illustrated in Fig.1. It is characterized by a DC power source, power switches, filters, and the parasitic capacitor  $C_{PV}$  between the PV panels and the grid ground. According to [4], the leakage current path is equivalent to an LC resonant circuit in

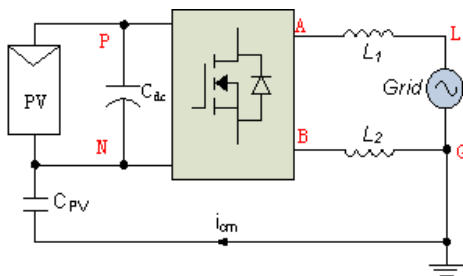


Fig.1 CM current path for the transformerless PV inverter

with the CM voltage. The equivalent common voltage  $u_{ecm}$  is defined as:

$$u_{ecm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{L_2 - L_1}{L_1 + L_2} \quad (1)$$

Where  $V_{AN}$  is the voltage difference between points A and N,  $V_{BN}$  is the voltage difference between points B and N, and  $L_1$  and  $L_2$  are the output filter inductors. Fig.2 shows the equivalent circuit for the CM current path.

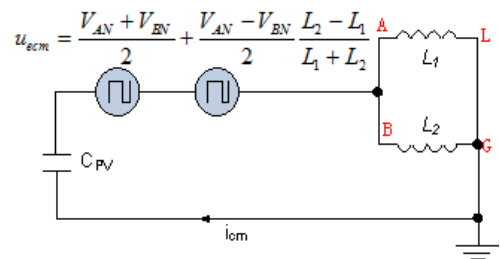


Fig.2 Equivalent circuit for the CM current path

To eliminate leakage currents, the CM voltage must be kept constant. When one inductor is working, such as in half bridge topologies [5] [6], the inductor  $L_2$  is zero. Therefore, (1) is simplified as:

$$u_{ecm} = \frac{V_{AN} + V_{BN}}{2} - \frac{V_{AN} - V_{BN}}{2} = V_{BN} \quad (2)$$

The drawback of half-bridge inverters is that the DC voltage utilization of half-bridge topologies is half of the full-bridge topologies, which means that large quantities of PV panels in series are required, or that a boost DC/DC converter with an extremely high voltage transfer ratio is necessary as the first power conditioning stage and system efficiency may be adversely affected. When two inductors are working where  $L_1$  is equal to  $L_2$ , the system is considered to have a symmetrical inductive structure. In this case, (1) is simplified as:

$$u_{cm} = \frac{V_{AN} + V_{BN}}{2} - 0 = \frac{V_{AN} + V_{BN}}{2} \quad (3)$$

From (3), the goal is keep the CM voltage constant for the full bridge topology. When compared to the bipolar SPWM, the unipolar SPWM has better performance in terms of the output current ripple and switching losses, though it cannot maintain a constant CM voltage. Instead, it generates the switching frequency CM voltage. For this reason, some state-of-the-art-topologies such as the H5 inverter, HERIC inverter, etc., have been developed from the symmetrical structure [7]-[9].

This paper is organized as follows: Section II describes the operation principles of the proposed method, Section III introduces all simplified topologies from MN principle, Section IV introduces non simplified topologies from MN principle, and Section V provides the results conclusions.

## II. OPERATION PRINCIPLES OF THE PROPOSED METHOD

Fig.3 shows the modulation for active power. The grid voltage and reference current are in phase. In the positive half period of the grid voltage, there are two operating modes for the inverter. Mode 1 is the positive conduction (PC) mode. The differential mode voltage  $V_{AB}$  is equal to input DC voltage. Mode 2 is the positive freewheeling (PF) mode. The differential mode voltage  $V_{AB}$  is equal to zero. In the negative half period of grid voltage, there are also two operating modes. Mode 3 is the negative conduction (NC) mode. Mode 4 is the negative freewheeling (NF) mode.

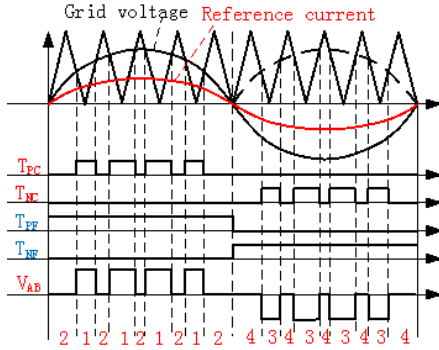


Fig.3 Modulation for active power

Fig.4 shows the full bridge topology and schematic diagram. The point P indicates the positive DC bus, point N indicates negative DC bus, point A indicates the first output of the bridge, and point B indicates the second output of the bridge. From Eq. (3), the CM voltage must be constant in order to minimize the leakage current. During PC and NC operating mode, the CM voltage is equal to half of the DC voltage and is a constant.

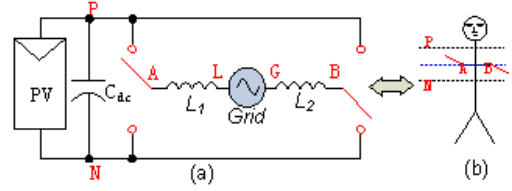


Fig.4 Full bridge (a) full bridge topology (b) schematic diagram of full bridge

Therefore, no leakage current will be generated. The common mode voltage should be kept to half of the DC voltage during PF and NF operating modes in order to minimize the leakage current. This provides an indication of how to construct inverter topologies which consistently minimize the leakage current. Fig.5 shows an illustration for the four desired operating modes of a full bridge inverter with minimized leakage current.

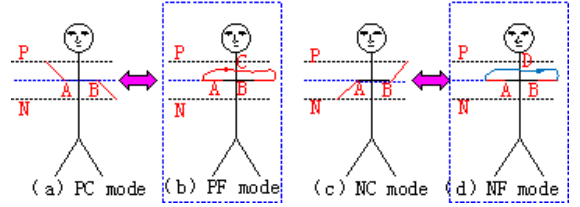


Fig.5 Four modes of improved full bridge (a) PC mode (b) PF mode (c) NC mode (d)NF mode

To best manage the leakage current, the inverter circuit should be constructed according to the following two criteria during PF and NF modes:

Firstly, all switches connected between the positive DC bus (P) and negative DC bus (N) must be off during the PF and NF intervals.

Secondly, it is necessary to provide the new controlled branch for PF mode and NF mode, such as branches C and D, as shown in Fig. 5(b) and (d).

In order to achieve these criteria, the mathematic analysis method called MN principle is been introduced.

It is assumed that  $M$  denotes to the total number of switches that are turned on during PC mode.  $X_1$  denotes the number of switches that connect point P to point A in PC mode and  $X_2$  denotes the number of switches that connect point B to point N in PC mode. Thus:

$$M = X_1 + X_2 \quad (4)$$

Similarly,  $N$  denotes the total number of switches that are turned on during NC mode.  $Y_1$  denotes the number of switches that connect point P to point B and  $Y_2$  denotes the number of switches that connect point A to point N during NC mode. Thus:

$$N = Y_1 + Y_2 \quad (5)$$

According to the criteria #1, during PF and NF operating mode, four switches should be off. They are the

switches between A and P, A and N, B and P and B and N. To acquire the simplified topology (ST), the maximum of the  $X_1, X_2, Y_1, Y_2$  shall be no more than 2. The detailed explain is introduced in Section IV.

$$\text{Max}(X_1, X_2, Y_1, Y_2) \leq 2 \quad (6)$$

When equation (6) is not satisfied, the topology is not the simplified topology, and the switches connected in series can be combined.  $Z_e$  is defined the simplified switch number. Therefore, only by using  $Z_e$  instead of  $Z$  according to the eq. (7) can the simplified topology be achieved.

$$Z_e = \begin{cases} Z & Z \leq 2 \\ 2 & Z > 2 \end{cases} \quad Z \in (X_1, X_2, Y_1, Y_2) \quad (7)$$

Tab.1 First family				Tab.2 Second family			
M:N	$X_1+X_2$	$Y_1+Y_2$		M:N	$X_1+X_2$	$Y_1+Y_2$	
2:2	1+1	1+1	M1	2:2	1+1	1+1	MD1
2:3	1+2	1+1	M2	2:3	1+2	1+1	MD2
	1+1	1+2		2:3	1+1	1+2	
3:2	2+1	1+1	M3	3:2	2+1	1+1	MD4
	1+1	2+1		3:2	1+1	2+1	
3:3	2+1	2+1	M4	3:3	2+1	2+1	MD4
	2+1	1+2	M5	3:3	2+1	1+2	✗
	1+2	2+1		3:3	1+2	2+1	✗
	1+2	1+2	M6	3:3	1+2	1+2	MD6
	2+1	3+1	△	3:3	2+1	3+1	✗
	3+1	2+1		3:3	3+1	2+1	✗
2+1	2+2	M7	3:3	2+1	2+2	✗	
2+2	2+1	△	3:3	2+2	2+1	✗	
2+1	1+3		3:3	2+1	1+3	✗	
3:4/4:3	1+3	2+1	△	3:4/4:3	1+3	2+1	✗
	1+2	3+1		3:4/4:3	1+2	3+1	
	3+1	1+2	△	3:4/4:3	3+1	1+2	✗
	1+2	2+2		3:4/4:3	1+2	2+2	
	2+2	1+2	M8	3:4/4:3	2+2	1+2	✗
	1+2	1+3	△	3:4/4:3	1+2	1+3	✗
1+3	2+1	3:4/4:3		1+3	2+1	✗	
4:4	2+2	2+2	MD9	4:4	2+2	2+2	MD7
4:4	others	△	4:4	others	✗or△		
3:5/5:3	all	△	3:5/5:3	all	✗or△		
4:5/5:4			4:5/5:4				

△--No simplified topologies ✗--No exist topology

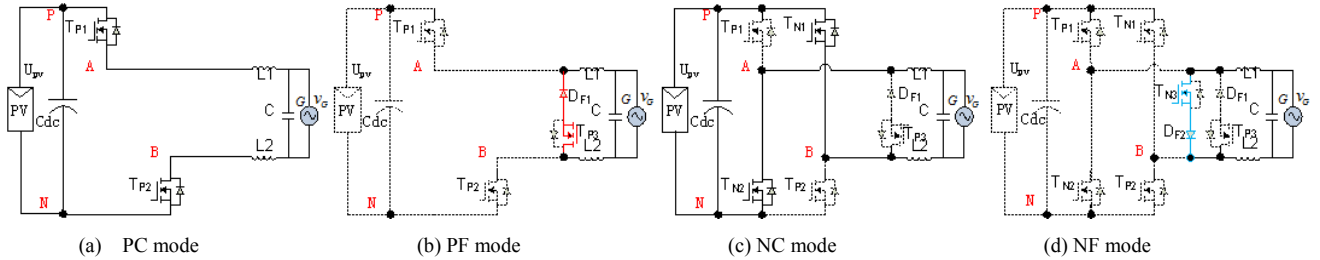


Fig.6 Four modes of M1 topology (a) PC mode (b) PF mode (c) NC mode (d) NF mode

### B. $M:N=3:3$

Fig.7 shows one example of the MD4 topology without external diodes. From table.2,  $X_1=2, X_2=1, Y_1=2, Y_2=1$ . In fig.7 (a), only two switches  $T_{p1}, T_{p2}$  are used between point P and point A as  $X_1=2$ . One switch  $T_{p3}$  is used between point B and point N as  $X_2=1$ . In fig.7 (b), the switches  $T_{p1}, T_{p3}$  are all off as all switches must stay off in

From Fig.5, the two controlled freewheeling branches should be added. Usually, this is achieved by using switch and a diode connected in series. Sometimes, the diode can be implemented by the body diode of an existing switch. Therefore, two topology families can be specified: one which uses external diodes and the other which appropriates the body diode of an existing switch. Table 1 shows the first topology family with external diodes. Table 2 shows the second topology family without external diodes.

### III. ALL SIMPLIFIED TOPOLOGIES FROM MN PRINCIPLE

In this section, several examples are provided to show how to use the MN principal to derive a bridge type inverter with minimal leakage currents. In this section, it is assumed that (6) is satisfied.

#### A. $M:N=2:2$ or $2:3$ or $3:2$

Fig.6 shows an example of the M1 topology with external diodes. From tab.1,  $X_1=1, X_2=1, Y_1=1, Y_2=1$ . In fig.6 (a), only one switch,  $T_{p1}$ , is used between point P and point A as  $X_1=1$ . One switch  $T_{p2}$ , is used between point B and point N as  $X_2=1$ . In fig.6 (b), the switches  $T_{p1}, T_{p2}$  are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switch  $T_{p3}$  and diode  $D_{F1}$  connects the point B and point A. In fig.6 (c), only one switch  $T_{N1}$  is used between point P and point B as  $Y_1=1$ . One switch  $T_{N2}$  is used between point A and point N as  $Y_2=1$ . In fig.6 (d), the switches  $T_{N1}, T_{N2}$  are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switch  $T_{N3}$  and diode  $D_{F2}$  connects the point A and point B. Similarly, the M2, M3 topology with external diodes and MD1, MD2, MD3 topology without external diodes can also be acquired.

freewheeling mode. The controlled branch using switch  $T_{p2}$  and diode  $D_{N2}$  connects the points B and A. In fig.7 (c), two switches  $T_{N1}, T_{N2}$  are used between point P and point B as  $Y_1=2$ . One switch  $T_{N3}$  is used between point A and point N as  $Y_2=1$ . In fig.7 (d), the switches  $T_{N1}, T_{N3}$  are keeping off as all switches must keep off in freewheeling mode. The controlled branch using switch  $T_{N2}$  and anti-diode  $D_{p2}$

connects the point A and point B. the topology can be simplified because the parallel switches  $T_{P1}$ ,  $T_{N1}$  can be instead of one switch  $T_1$ . Similar analysis, the M4, M5, M6

topologies with external diodes and MD6 without external diodes are also be acquired.

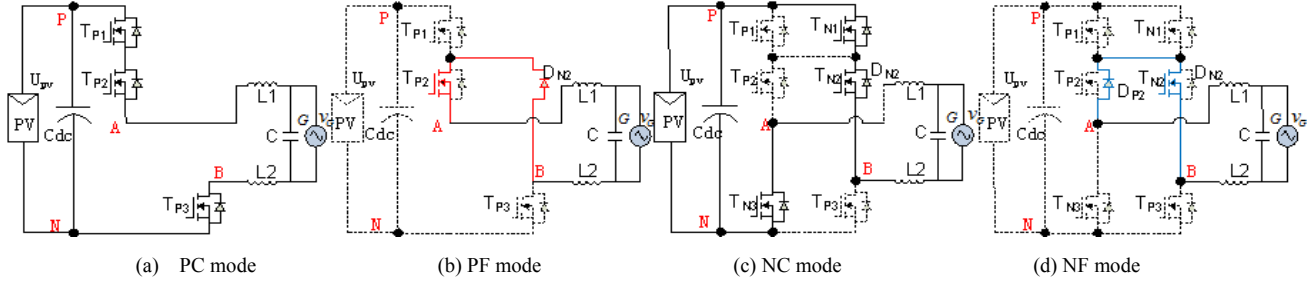


Fig.7 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

C.  $M:N=3:4$  or  $4:3$

Fig.8 shows an example of the M8 topology with external diodes. From table.1,  $X_1=1$ ,  $X_2=2$ ,  $Y_1=2$ ,  $Y_2=2$ . In fig.8 (a), one switch  $T_{P1}$  is used between point P and point A as  $X_1=1$ . Two switches  $T_{P2}$  and  $T_{P3}$  are used between point B and point N as  $X_2=2$ . In fig.8 (b), the switches  $T_{P1}$ ,  $T_{P3}$  remain off as all switches must again stay off in freewheeling mode. The controlled branch using switch  $T_{P2}$

and diode  $D_{F1}$  connects point B and point A. In fig.9 (c), two switches,  $T_{N1}$  and  $T_{N2}$ , are used between point P and point B as  $Y_1=2$ . Two switches  $T_{N3}$ ,  $T_{N4}$  are used between point A and point N as  $Y_2=2$ . In fig.9 (d), the switches  $T_{N1}$  and  $T_{N4}$  remain off as they must in freewheeling mode. The controlled branch using switches  $T_{N2}$  and  $T_{N3}$ , and anti-diodes  $D_{P2}$  and  $D_{P3}$  connects points A and B. Similarly, the MD6 without external diodes can also be acquired.

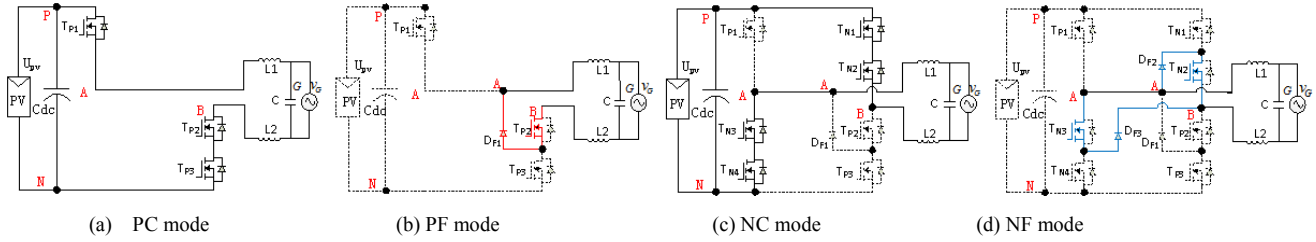


Fig.8 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

D.  $M:N=4:4$

Fig.9 shows an example of the M8 topology with external diodes. From table.1,  $X_1=2$ ,  $X_2=2$ ,  $Y_1=2$ ,  $Y_2=2$ . In fig.9 (a), switches  $T_{P1}$  and  $T_{P2}$  are used between point P and point A as  $X_1=2$ . Two switches  $T_{P3}$ ,  $T_{P4}$  are used between point B and point N as  $X_2=2$ . In fig.9 (b), the switches  $T_{P1}$ ,  $T_{P4}$  again remain off as all expected in freewheeling mode. The controlled branch using switches  $T_{P2}$  and  $T_{P3}$ , as well as diodes  $D_{N2}$  and  $D_{N3}$  connect the

points B and A. In fig.9 (c), two switches  $T_{N1}$  and  $T_{N2}$  are used between point P and point B as  $Y_1=2$ . Two switches  $T_{N3}$ ,  $T_{N4}$  are used between point A and point N as  $Y_2=2$ . In fig.9 (d), the switches  $T_{N1}$  and  $T_{N4}$  remain off as all switches stay keep off in freewheeling mode. The controlled branch using switch  $T_{N2}$ ,  $T_{N3}$  and anti-diode  $D_{P2}$ ,  $D_{P3}$  connects point A and point B. This topology can be simplified. The parallel switches  $T_{P1}$  and  $T_{N1}$  can be instead of one switch  $T_1$ . Similarly, the parallel switches  $T_{P4}$  and  $T_{N4}$  can also become the single switch  $T_4$ .

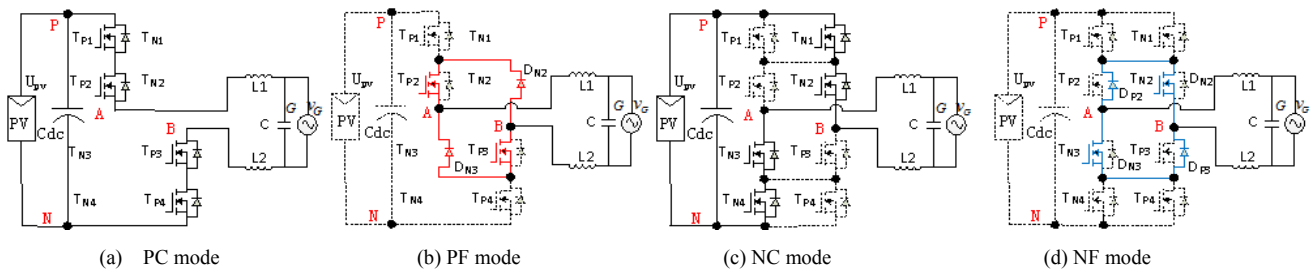


Fig.9 Four modes of MD2 topology (a) PC mode (b) PF mode(c) NC mode (d) NF mode

E. All simplified topology from MN principle

From the above described analysis method, we may generate the following simplified topologies using the MN principle, as shown in Fig.10 [10]-[16].

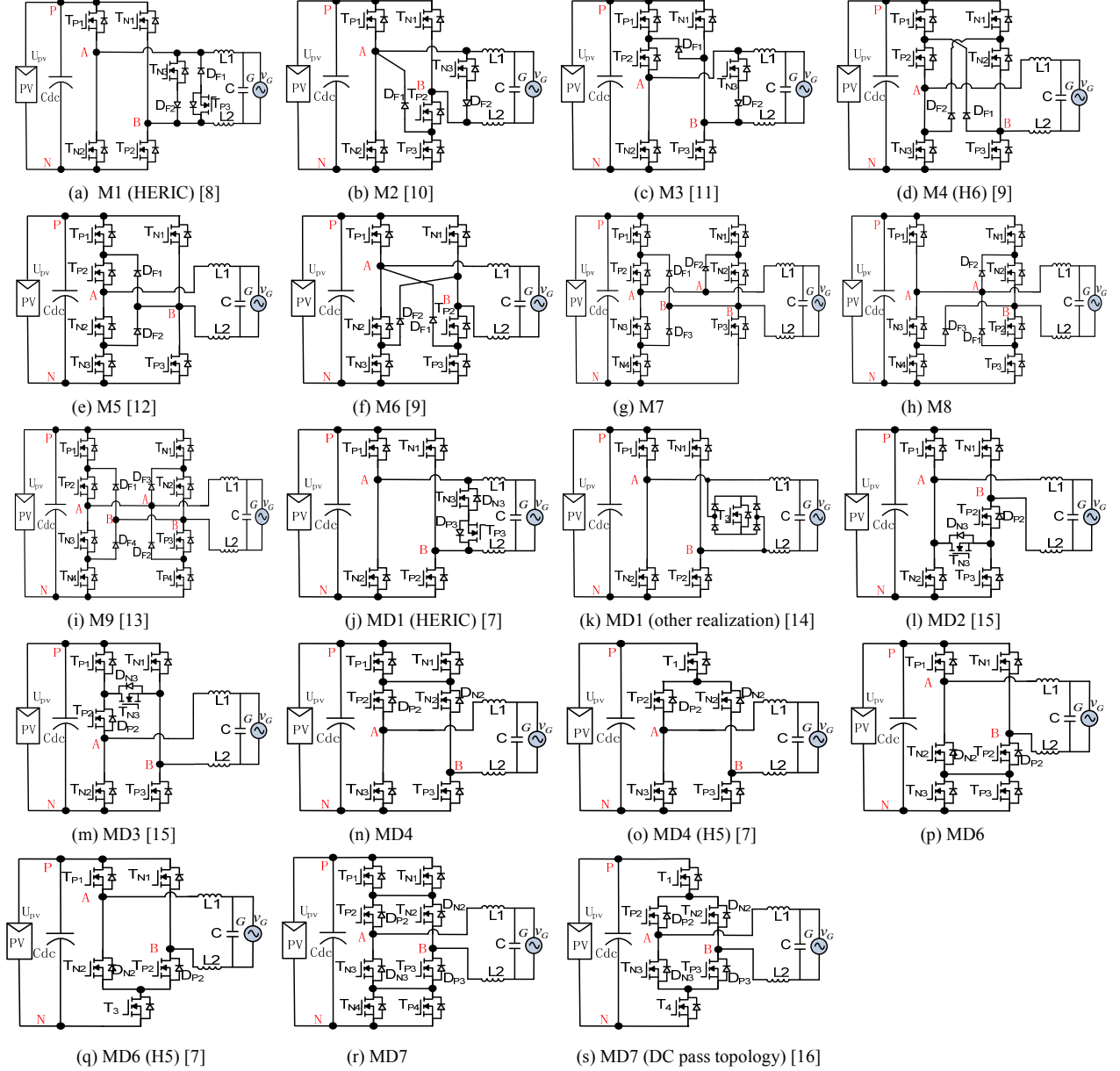


Fig.10 All simplified topology from MN principle

IV. NON SIMPLIFIED TOPOLOGIES FROM MN PRINCIPLE

In this section, several examples are given to show how to use the MN principal to derive a bridge type inverter with minimum leakage current. This time, it is assumed that (6) is not satisfied. Therefore, the following demonstrated topologies are not the most in their most simplified forms.

A.  $M:N=3:4$  or  $4:3$

Despite this, we can generate many new topologies from the MN principle. However, in this case some series switches can be combined as necessary. The simplified topologies are that use the  $Z_c$  instead of  $Z$  according to the Eq. (7).

For example, For  $M=3$   $N=4$  (or  $M=4$   $N=3$ ), there also are four combined types. First,  $X_1=1$ ,  $X_2=2$ ,  $Y_1=3$ ,  $Y_2=1$ .



Second,  $X_1=1, X_2=2, Y_1=1, Y_2=3$ . Third,  $X_1=2, X_2=1, Y_1=3, Y_2=1$ . Fourth,  $X_1=2, X_2=1, Y_1=1, Y_2=3$ .

Fig.11 shows one example of  $X_1=2, X_2=1, Y_1=3, Y_2=1$ . Obviously, the switches between  $T_{N2}, T_{N3}$  can be

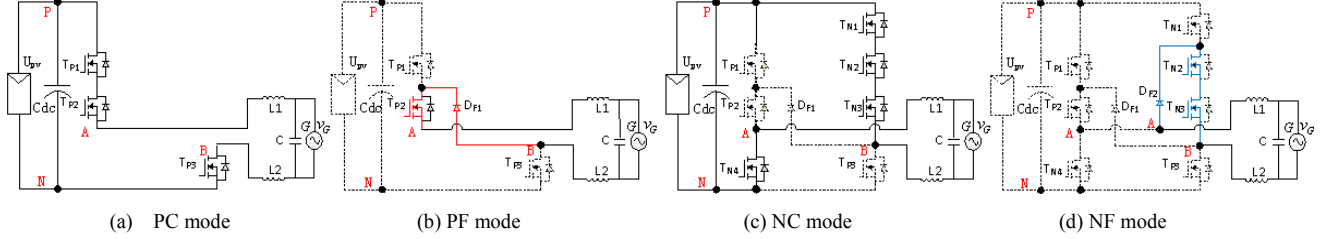


Fig.11 First topology of  $X_1=1, X_2=2, Y_1=3, Y_2=1$  (a) PC mode (b) PF mode (c) NC mode (d) NF mode

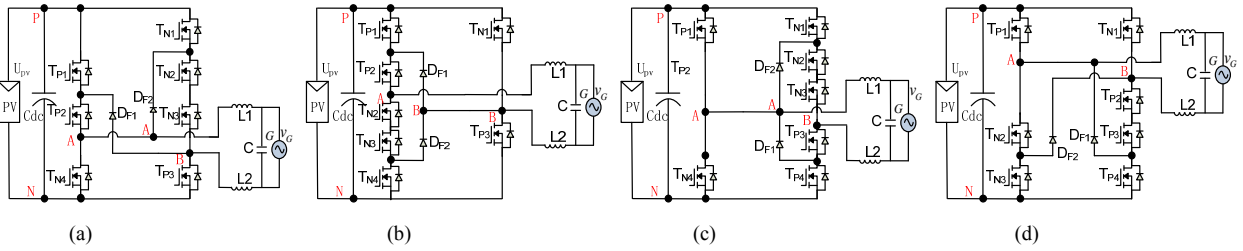


Fig.12 Four topologies of  $M=3 N=4$  or  $M=4 N=3$  (a)  $X_1=1, X_2=2, Y_1=3, Y_2=1$  (b)  $X_1=1, X_2=2, Y_1=1, Y_2=3$  (c)  $X_1=2, X_2=1, Y_1=3, Y_2=1$  (d)  $X_1=2, X_2=1, Y_1=1, Y_2=3$

#### B. $M:N= 3:5$ or $5:3$ or $4:5$ or $5:3$ and so on

When  $M$  or  $N$  is more than 4, such as  $M=5$ , the  $X_1$  or  $X_2$  is more than 2. The new topologies include the redundant switches. Their simplified topologies are seen in Fig.10.

For example, When the  $X_1=2, X_2=1, Y_1=1, Y_2=4$ , the  $Y_2$  is more than 2, the  $Y_2$  is instead of  $Y_{e2}$  according to the Eq. (7). The simplified topology is  $X_1=2, X_2=1, Y_1=1, Y_{e2}=2$ , and it is equivalent to  $M5$  topology shown in Fig.10 (e).

#### V. CONCLUSION

The MN synthesis method is proposed to derive new full bridge inverter with minimum leakage current introduced by common mode voltage. The MN method has two primary criteria. Additionally, examples have been provided to illustrate how to use the MN principal to derive new topologies. It has been demonstrated that there are only 15 full bridge inverter topologies that can minimize the leakage current. The final paper will provide a more detailed analysis and derivation procedure of this method. The two basic criteria shall be seen in more detail, as well as a rigorous analysis of the simplified topologies. Here, 15 simplified topologies have been synthesized according to the MN method. All other possible topologies have been shown to be the non-simplified equivalents, depending on the existence and requirements of external diodes. This paper has also introduced the method to simplify the non-simplified topologies. We have has proven that no new simplified full bridge topologies exist. Notably, most of the simplified topologies from MN method have been verified by existing papers and patents.

instead of one switch. Thus, the simplified topology is  $M4$  shown in Fig.10 (d). Fig.12 shows the four non-simplified topologies. Their simplified topologies are  $M4, M5, M5,$  and  $M6$  shown in Fig.10 (d), (e), (f).

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