A New Resonant Gate-Drive Circuit With Efficient Energy Recovery and Low Conduction Loss

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***Abstract*—In this paper, a new resonant gate-drive circuit is proposed to recover a portion of the power-MOSFET-gate energy that is typically dissipated in high-frequency converters. The proposed circuit consists of four control switches and a small resonant inductance. The current through the resonant inductance is discontinuous in order to minimize circulating-current conduction loss that is present in other methods. The proposed circuit also achieves quick turn-on and turn-off transition times to reduce switching and conduction losses in power MOSFETs. An analysis, a design procedure, and experimental results are presented for the proposed circuit. Experimental results demonstrate that the proposed driver can recover 51% of the gate energy at 5-V gate-drive voltage.**

***Index Terms*—Gate drive, gate-energy recovery, gate loss, MOSFET gate drive, MOSFET gate driver, resonant gate drive, resonant gate driver.**

I. Introduction

POWER MOSFETs operate with gate loss that is equal to the product of the total gate charge, gate-drive voltage, and switching frequency as given by

$$P_{\text{gate}} = Q_g V_{\text{GS}} f_S. \tag{1}$$

Traditionally, in low-power converters operating at switching frequencies below 500 kHz, gate loss was considered to be small in comparison to other losses. However, in recent years, as switching frequencies have increased above 500 kHz and MOSFETs with lower R_{DS} ratings have been used, gate losses have increased enough that there has been a push to develop techniques to recover some, or all, of the gate energy in low-power dc–dc converters.

Resonant gate-drive techniques provide a promising method to reduce gate loss in many types of dc–dc converters [1]–[6] to enable higher efficiency or higher frequency operation. Since the early 1990s, there has been a significant amount of work published for dc–dc converters operating above 1 MHz, and several papers and patents have been published, proposing techniques to recover gate energy [7]–[20].

After reviewing these drivers, it can be concluded that it is desirable to design a resonant driver with the following three characteristics.

1) Minimal circulating current in order to minimize conduction loss in the driver circuit during the power-MOSFET ON and OFF states. However, the drivers proposed in [8]–[11] operate with a continuous inductor current to achieve a nearly constant current gate drive at the expense of high conduction loss in the driver.
2) Quick turn-on and turn-off transition times to minimize both conduction and switching losses in the power MOSFET. The drivers proposed in [12]–[20] all operate with low circulating current; however, they also operate with slow turn on and/or turn off since the inductor or transformer current begins to charge/discharge the MOSFET gate from zero.
3) The ability to actively clamp the power-MOSFET gate to the gate-drive supply during the on time and to ground during the off time in order to avoid undesired false triggering of the power-MOSFET gate, i.e., $Cd\nu/dt$ immunity. However, the drivers proposed in [12]–[14], [17], [19], and [20] do not clamp the power-MOSFET gate with a low-impedance switch, so the potential for $Cd\nu/dt$ false triggering exists.

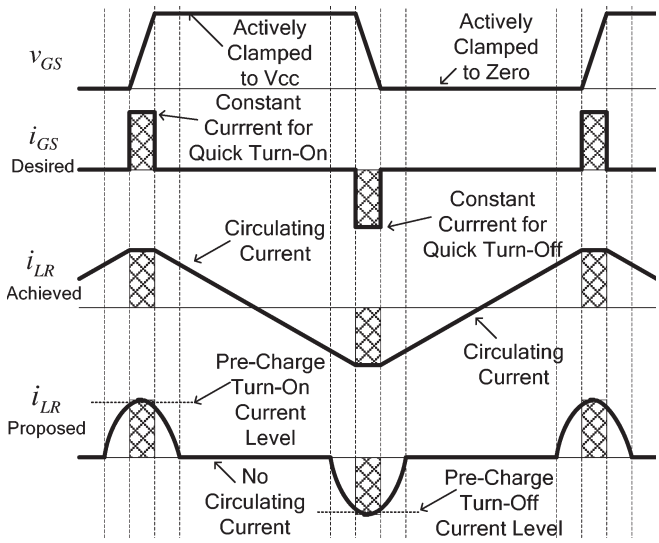

Fig. 1. Evolution of the proposed resonant gate-drive circuit.

Conventional lossy gate-drive methods use a voltage source to charge and discharge the power-MOSFET gate through a resistive switch and an external resistor. Energy is taken from the gate-drive supply to charge the gate and then sent to ground when discharging the gate. A bidirectional current pulse wave can also be used to drive the gate. This is shown in Fig. 1 by the second curve $i_{\text{GS Desired}}$. To achieve lossless gate drive, the gate energy must be returned to the gate-drive supply, which can be accomplished by using an inductor as temporary storage.

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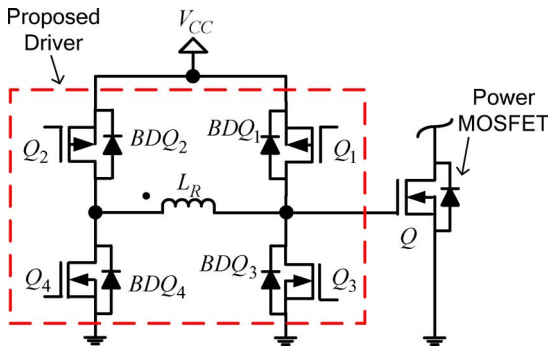

Fig. 2. Proposed resonant gate-drive circuit.

Conveniently, an inductor can also be used as a current source to drive the gate. However, the inductor current cannot step to achieve the desired gate current source, so in the method proposed in [7], the inductor current is a continuous one that is triangular in shape, as shown by the $i_{\mathrm{LR\,Achieved}}$ curve in Fig. 1.

Other previously proposed resonant gate-drive methods allow the inductor current to go discontinuous. However, they suffer from slow transition times since the power-MOSFET-gate capacitance begins to charge when the inductor current starts at zero. Therefore, if it is possible to combine the benefits of the two methods, namely, discontinuous inductor current and relatively constant drive current in [7], then an optimal resonant gate driver can be achieved. This idea is presented in the curve labeled $i_{\mathrm{LR\,Proposed}}$ in Fig. 1. Because the inductor current cannot step, a charging interval is used so that the current reaches a precharge turn-on level before directing the current to the gate. After charging the power-MOSFET gate, this current can then be allowed to decrease while, at the same time, clamping the gate high. This idea can be implemented as shown in Section II. The driver logic is presented in Section IV. A design procedure and a design example are presented in Sections V and VI, respectively. The impact of R_G and other practical issues are presented in Section VII. Experimental results are presented in Section VIII, and conclusions are presented in Section IX.

II. Proposed Circuit and Waveforms

A circuit is shown in Fig. 2, which can achieve the desired inductor-current wave shape $i_{\mathrm{LR\,Proposed}}$ in Fig. 1. The circuit consists of four control switches and one small inductor. Switch Q represents the power MOSFET to be driven.

Figs. 3–5 can be used to explain the operation of the circuit in order to understand how the gate energy can be saved. The current paths during the four intervals of the turn-on stage are shown in Fig. 3. The current paths during the four intervals of the turn-off stage are shown in Fig. 4. The gating waveforms of the four control switches Q_1–Q_4, along with the inductor current, gate current, power-MOSFET gate-to-source voltage, and gate-drive supply current, are shown in Fig. 5. It is noted that Q_1 and Q_2 are P-channel MOSFETs, so their control signals are active low. The ON state for the four gating signals of Q_1–Q_4 are shaded in Fig. 5.

The operation of the circuit is explained as follows. Initially, it is assumed that the power MOSFET is in the ON state before

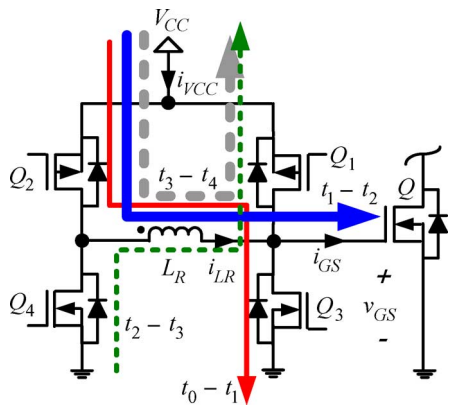

Fig. 3. Current paths during the turn-on intervals.

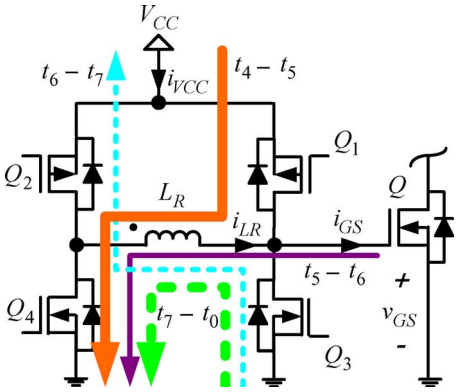

Fig. 4. Current paths during the turn-off intervals.

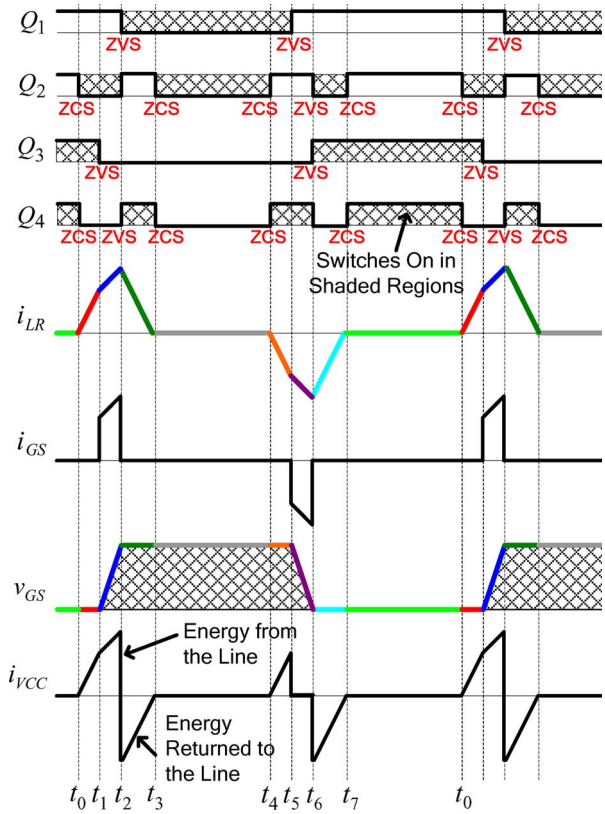

Fig. 5. Proposed resonant gate-drive-circuit waveforms. Q_1–Q_4 are the gating waveforms for control MOSFETs Q_1–Q_4, with the shaded regions representing the ON states.

time t_0; only switches Q_3 and Q_4 are on, and the gate of Q is clamped to 0 V. In all cases, a small dead time (not shown) is added between the complementary transitions of Q_2 and Q_4 to eliminate shoot-through and allow zero-voltage switching (ZVS) or zero-current switching (ZCS).

1) t_0–t_1*:* At time t_0, Q_4 turns off (with ZCS), and then Q_2 turns on (with ZCS), allowing the inductor current to ramp up. The current path during this interval is $Q_2{-}L_R{-}Q_3$. Because Q_3 is in the ON state, the gate of Q is clamped low. The interval ends at time t_1.

2) t_1–t_2*:* At time t_1, Q_3 turns off (with approximate ZVS due to large shunt power-MOSFET-gate capacitance), which allows the inductor current to begin to charge the power-MOSFET gate. Because the dotted side of the inductor is clamped to the gate drive supply and the other side is connected to the gate capacitance of Q, the inductor current will continue to ramp up but with a reduced slope as the voltage across the gate capacitance increases. The current path during this interval is $Q_2{-}L_R{-}C_G$, where C_G represents the equivalent gate capacitance of Q. This interval ends at time t_2, when $\nu_{\rm GS}$ reaches $V_{\rm CC}$. If this interval is allowed to continue, the body diode of switch Q_1 will allow the current to freewheel through $Q_2{-}L_R{-}BDQ_1$.

3) t_2–t_3*:* At time t_2, Q_2 turns off, and Q_1 and then Q_4 turn on (both with ZVS), allowing the inductor current to conduct into the dot through the path $Q_4{-}L_R{-}Q_1$. Most importantly, it is during this interval when the gate charging energy is returned to the gate-drive supply. This can be observed from the negative portion of the $i_{\rm VCC}$ curve in Fig. 5. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down toward zero. During this interval, the gate voltage of Q remains clamped to the gate-drive supply voltage $V_{\rm CC}$. The interval ends when the inductor current reaches zero at time t_3.

4) t_3–t_4*:* At time t_3, Q_4 turns off (with ZCS), and then Q_2 turns on (with ZCS), which allows any residual inductor current to freewheel through $Q_2{-}L_R{-}Q_1$. During this interval, the gate voltage of Q remains clamped to $V_{\rm CC}$. The interval ends at time t_4, when the precharging interval for the turn-off cycle begins as dictated by the pulsewidth-modulation (PWM) signal.

5) t_4–t_5*:* At time t_4, the turn-off precharging interval begins. Q_2 turns off (with ZCS), and Q_4 turns on (with ZCS). Because Q_1 was previously on, the inductor current begins to ramp negative out of the dot through the path $Q_1{-}L_R{-}Q_4$. During this interval, the gate voltage of Q remains clamped to $V_{\rm CC}$. The interval ends at time t_5.

6) t_5–t_6*:* At time t_5, Q_1 turns off (with shunted ZVS from Q), which allows the inductor current to begin to discharge the power-MOSFET gate. Because the dotted side of the inductor is clamped to ground and the other side is connected to the gate capacitance of Q, the inductor current will continue to ramp negative but with a reduced slope as the voltage across the gate capacitance decreases. The current path during this interval is $C_G{-}L_R{-}Q_4$, where C_G represents the equivalent gate capacitance of Q. This interval ends at time t_6, when ν_{GS} reaches zero. If this interval is allowed to continue, the body diode of switch Q_3 will allow the current to freewheel through $BDQ_3{-}L_R{-}Q_4$.

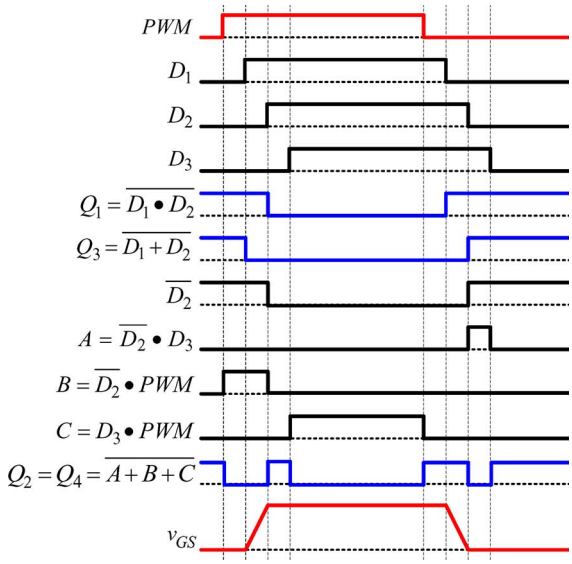

Fig. 6. Logic waveforms used to create the control-switch gating signals for Q_1–Q_4.

7) t_6–t_7*:* At time t_6, Q_4 turns off, and Q_2 and Q_3 turn on (both with ZVS), allowing the inductor current to conduct out of the dot through the path $Q_3{-}L_R{-}Q_2$. Most importantly, it is during this interval when the gate discharging energy is returned to the gate-drive supply. This can be observed from the negative portion of the $i_{\rm VCC}$ curve in Fig. 5. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive toward zero. During this interval, the gate voltage of Q remains clamped to ground. The interval ends when the inductor current reaches zero at time t_7.

8) t_7–t_0*:* At time t_7, Q_2 turns off (with ZCS), and Q_4 turns on (with ZCS), which allows any residual inductor current to freewheel through $Q_3{-}L_R{-}Q_4$. During this interval, the gate voltage of Q remains clamped to ground. The interval ends at time t_0 when the precharging interval begins and the entire process repeats as dictated by the PWM signal.

It can be observed from the operating intervals that energy is taken from the gate-drive supply during the following three intervals: t_0–t_1, t_1–t_2, and t_4–t_5, and energy is returned to the gate-drive supply during the following two intervals: t_2–t_3 and t_6–t_7. Qualitatively, if the positive and negative amp–second area products are equal, then all of the gate energy can be recovered. However, because the real circuit will have losses in the control switches, control-switch predrivers, inductor, and power-MOSFET-gate resistance, all of the gate energy cannot be recovered, so the positive amp–second area will be greater than the negative amp–second area.

III. Logic Implementation

The logic required to produce the gating signals for the four control switches Q_1–Q_4 is very simple. The logic waveforms used to create the three control signals for Q_1–Q_4 are shown in Fig. 6. The only logic input to the gate-drive circuit is a PWM signal generated by the converter controller. In order to implement the appropriate precharging intervals, gate charging intervals, and energy return intervals, delay circuitry is required

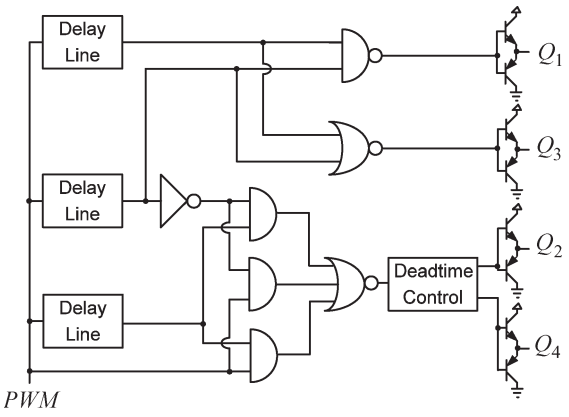

Fig. 7. Logic circuit used to create the control-switch gating signals for Q_1–Q_4.

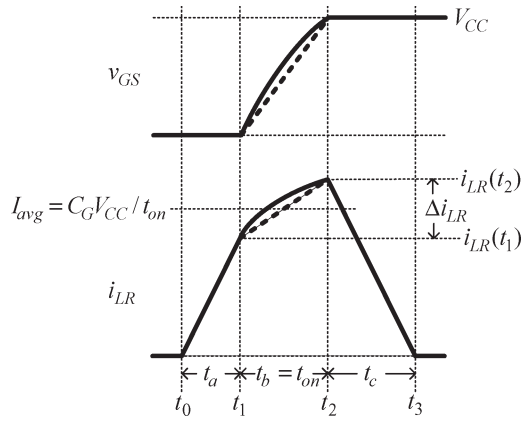

Fig. 8. Detailed inductor-current waveform and power-MOSFET gate voltage during the turn-on interval.

to delay the PWM signal for the appropriate times. The delayed signals are labeled D_1–D_3. The required gating signals for Q_1–Q_4 are given after the PWM signal using the logic functions labeled A–C.

The logic circuit used to create the three control signals for Q_1–Q_4 is shown in Fig. 7. Tapped delay lines can be used for the delay elements. High-speed gates should be used for the logic elements. The predrivers consist of bipolar-junction-transistor totem-pole pairs. Dead-time control is not needed for Q_1 and Q_3 because the logic creates a delay between their gating signals.

IV. Loss Analysis

The sources of loss in the proposed driver include conduction losses in the driver switches, inductor, and MOSFET-gate resistance. In comparison to a conventional gate driver with two switches, the proposed resonant gate driver exhibits inductor core loss and additional gate loss in the extra two switches Q_2 and Q_4 in the left leg, which switch at three times the switching frequency. There is no additional switching loss in the proposed driver. In fact, because the right-leg switches with ZVS at turn on, some additional energy is saved in comparison to a conventional driver.

This section will focus on the conduction loss in the driver switches. The additional gate loss in Q_2 and Q_4 can be easily calculated by using (2), where Q_{G2} and Q_{G4} represent the total gate charge in switches Q_2 and Q_4, respectively. Given this additional gate loss at three times the switching frequency, it is noted that switches Q_2 and Q_4 should be chosen to minimize both their conduction loss and additional gate loss, so it is reasonable to assume that they can be selected with lower gate charge and higher on resistances than Q_1 and Q_3

$$P_{GQ2Q4} = 3f_S(Q_{G2} + Q_{G4})V_{\rm CC}. \tag{2}$$

In order to calculate conduction loss in the driver, the power MOSFET being driven is represented by an RC network consisting of its parasitic series gate resistance R_G and an equivalent gate capacitance $C_G = Q_G/V_{\rm CC}$ which is easily calculated by using the total gate-charge data from the device datasheet. During the ON state, the control switches can be represented by series resistances $R_1 - R_4$. The inductor copper loss can be represented by an equivalent series resistance R_L which can be estimated or obtained from the datasheet.

The conduction loss in the proposed resonant gate driver can be determined by analyzing the losses during the three main states of the turn-on interval. This is clear because the turn-off interval is symmetrical with respect to the turn-on interval, so the turn-on losses can be doubled.

The detailed inductor-current and power-MOSFET gate-voltage waveforms are shown for the turn-on interval in Fig. 8. The actual inductor-current waveform will follow the shape given by the solid line with a nonlinear transition during the turn on of the gate voltage. Using a piecewise-linear approximation to simplify the analysis, the inductor-current waveform can be approximated using the dotted portion during $t_{\rm on}$, so that the entire interval is given by the shaded region. The power-MOSFET-gate voltage will follow the solid line during turn on but can be approximated by the dotted line if it is assumed that the gate is driven by a constant current source of value $I_{\rm avg}$ during $t_{\rm on}$.

In Fig. 8, the inductor-current precharge interval is labeled t_a, and it occurs from time t_0 to t_1. The actual turn-on interval is labeled t_b, which is also $t_{\rm on}$, and it occurs from time t_1 to t_2. The ramp-down interval is labeled t_c, and it occurs from t_2 to t_3.

It is useful to derive a few relationships before explaining the three intervals in greater detail. The first requirement is to determine or set the turn-on time $t_{\rm on}$ of the power MOSFET. This is usually dictated by the application. Once $t_{\rm on}$ is set, using the piecewise-linear approximation during the t_b interval, the average inductor current is derived by using (3), which is simplified to (4) in order to determine $I_{\rm avg}$

$$Q_G = I_{\rm avg} t_{\rm on} = C_G V_{\rm CC} \tag{3}$$

$$I_{\rm avg} = \frac{Q_G}{t_{\rm on}}. \tag{4}$$

In order to simplify the analysis, it is useful to define the transition time $t_{\rm on}$ as a fraction of the switching period. By using F to denote the selected fraction of the switching period, $t_{\rm on} = F/f_S$.

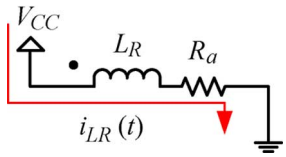

Fig. 9. Equivalent circuit during the precharge interval t_a.

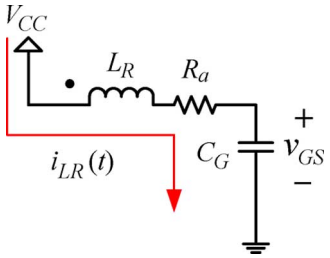

Fig. 10. Equivalent circuit during the turn-on transition interval t_b.

The final useful relationship is to express the ripple portion of the inductor current during $t_{\rm on}$. The actual equivalent circuit is complex, but because the power-MOSFET-gate capacitor voltage increases from zero to $V_{\rm CC}$ during $t_{\rm on}$, then the average capacitor voltage during the interval is $V_{\rm CC}/2$. By using this approximation, the ripple-current component $\Delta i_{\rm LR}$ can be approximated using

$$\Delta i_{\rm LR} = \frac{V_{\rm CC}}{2}\frac{F}{f_S}\frac{1}{L_R}. \tag{5}$$

The analysis of the three intervals is explained as follows.

1) t_a: The equivalent circuit during t_a is shown in Fig. 9. During this interval, switches Q_2 and Q_3 are on, so the circuit is a series RL circuit consisting of R_2, R_L, R_3, and L_R, where the resistances R_2, R_L, and R_3 have been lumped together as R_a $(R_a = R_2 + R_L + R_3)$. Because the inductor value ultimately determines the duration of the three turn-on transition time intervals and the ripple current $\Delta i_{\rm LR}$, it is useful to express the power consumption P_a as a function of the inductor value. It can be shown that t_a and P_a can be expressed as

$$t_a = \frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} - \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right] \tag{6}$$

$$P_a = \frac{f_S}{3}R_a\frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} - \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right]^3. \tag{7}$$

2) t_b: The equivalent circuit during t_b is shown in Fig. 10. During this interval, only switch Q_2 is on, so the circuit is a series RLC circuit consisting of R_2, R_L, R_G, L_R, and C_G, where the resistances R_2, R_L, and R_G have been lumped together as R_b $(R_b = R_2 + R_L + R_G)$. It can be shown that the power consumption P_b during the interval is given by

$$P_b = FR_b\left[\left(\frac{f_S Q_G}{F}\right)^2 + \frac{1}{12}\left(\frac{V_{\rm CC}F}{2f_S L_R}\right)^2\right]. \tag{8}$$

3) t_c: The equivalent circuit during t_c is shown in Fig. 11. During this interval, switches Q_4 and Q_1 are on, so the circuit is a series RL circuit consisting of R_4, R_L, R_1, and L_R, where

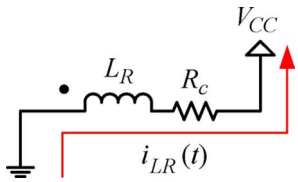

Fig. 11. Equivalent circuit during the ramp-down interval t_c.

the resistances R_4, R_L, and R_1 have been lumped together as R_c $(R_c = R_4 + R_L + R_1)$. The power consumption during the interval is given by (9). The time interval t_c can be expressed as

$$P_c = \frac{f_S}{3}R_c\frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} + \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right]^3 \tag{9}$$

$$t_c = \frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} + \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right]. \tag{10}$$

The total conduction loss in the proposed resonant gate-drive circuit is two times (turn on and off) the sum of P_a plus P_b plus P_c, as given by (11). The energy recovery of the proposed resonant gate driver is given by

$$\begin{aligned} P_{\rm cond} =& 2\frac{f_S}{3}R_a\frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} - \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right]^3 \\ &+ 2FR_b\left[\left(\frac{f_S Q_G}{F}\right)^2 + \frac{1}{12}\left(\frac{V_{\rm CC}F}{2f_S L_R}\right)^2\right] \\ &+ 2\frac{f_S}{3}R_c\frac{L_R}{V_{\rm CC}}\left[\frac{Q_G f_S}{F} + \frac{V_{\rm CC}}{4}\frac{F}{f_S}\frac{1}{L_R}\right]^3 \end{aligned} \tag{11}$$

$$\eta_{\rm rec} = \left[1 - \frac{P_{\rm cond} + P_{GQ2Q4}}{P_{\rm gate}}\right]. \tag{12}$$

V. Design Procedure

The first step in the design procedure is control-switch selection. The control switches should be selected in order to minimize conduction loss while, at the same time, minimizing gate loss. The left-leg switches Q_2 and Q_4 should be selected with lower gate charge than the right-leg switches Q_1 and Q_3.

The goal of the design procedure is to minimize the conduction loss in the proposed circuit, which is accomplished through proper selection of the inductor. If the inductor is too small, the L/R time constant will not be large enough, and the inductor energy storage will not be sufficient. Furthermore, the peak current during $t_{\rm on}$ will be too large. On the other hand, if the inductor is too large, there is excess conduction loss during the on and off times of the power MOSFET. Mathematically, this behavior can be observed in (11), which is a function of $(1/L_R)^2 + L_R$, which, as a function of L_R, contains a minimum value. The minimum value can be easily found by differentiating (11) with respect to L_R, setting the result to be equal to zero and then solving for the real and positive value of L_R. This value of inductance is given by (13), shown at the bottom of the next page, which can be evaluated by using a mathematical software package for the given operating point.

TABLE I
SWITCH PARAMETERS FOR THE RESONANT GATE DRIVER

Label	Part #	R_{DS}@ V_{GS}=5V [Ω]	Q_G@ V_{DS}=0V [nC]	Q_G@ V_{DS}=5V [nC]	R_G [Ω]
Q	IRF6691	NA	2(40) =80 (Q_G)	NA	0.6/2=0.3 (R_G)
Q_1	FDN342P	0.06 (R_1)	NA	6.5 (Q_{G1})	NA
Q_3	FDN335N	0.06 (R_3)	NA	1.75 (Q_{G3})	NA
Q_2	FDN358P	0.15 (R_2)	NA	3.5 (Q_{G2})	NA
Q_4	NDS351AN	0.09 (R_4)	NA	1.25 (Q_{G4})	NA

TABLE II
ADDITIONAL CIRCUIT PARAMETERS FOR THE RESONANT GATE DRIVER

Label	Value
V_{CC}	5V
F	0.1
f_S	1.5MHz
R_L	0.05Ω
R_a	R_2+R_L+R_3=0.26Ω
R_b	R_2+R_L+R_G=0.5Ω
R_c	R_4+R_L+R_1=0.29Ω

After calculating the optimal inductor value, shown in (13), the delay times t_a, t_b, and t_c should be calculated by using (4), (6), and (10), respectively, in order to determine the required delay times for the logic.

VI. DESIGN EXAMPLE

A switching power converter is designed to operate at 1.5 MHz to deliver power to a 35-A load at 1 V. Two pairs of synchronous-rectifier (SR) power MOSFETs are used in the rectifier stage. The SRs are driven by a 5-V source. The power MOSFET Q and control switches Q_1–Q_4 were selected, and their relevant parameters are given in Table I. The turn-on transition time was selected to be 10% of the switching period, corresponding to $F = 0.1$. The control switches were selected with the guideline that their gate charge should be less than 10% of that for the power MOSFET being driven. In addition, minimal $R_{\rm DS}$ devices were desired to minimize conduction loss in the driver circuit (the goal in selection was to keep the $R_{\rm DS}$ below 500 mΩ). The tradeoff in the selection process is between gate charge and $R_{\rm DS}$. Because Q_2 and Q_4 switch at three times the switching frequency, lower gate-charge and higher $R_{\rm DS}$ devices were selected in comparison to Q_1 and Q_3.

Using the parameters in the tables along with (13), the optimal inductance value is $L_R = 170$ nH. Rounding to the nearest 5 ns, the required transition times were calculated to be $t_a = 25$ ns using (6), $t_b = t_{\rm on} = 65$ ns using (4), and $t_c = 55$ ns using (10), corresponding to the required delay times of $t_1 = 25$ ns (t_a), $t_2 = 95$ ns $(t_a + t_b)$, and $t_3 = 155$ ns $(t_a + t_b + t_c)$ for the PWM signal. Circuit parameters used to calculate the optimal inductance value and conduction loss are summarized in Table II.

The total conduction loss in the driver is 188 mW, which is calculated by using (11). The additional gate loss attributed to Q_2 and Q_4 is 107 mW, which is calculated by using (2), for a total driver loss of 295 mW. There is no additional switching loss in the proposed driver in comparison to a conventional driver because Q_1 and Q_3 switch with ZVS. Since two drive circuits are required for the converter because there are two pairs of SRs, the total-conduction-loss and additional-gate-loss quantities are doubled and therefore become 376 and 214 mW, respectively. The total loss using the proposed method would be 590 mW. The total gate loss using conventional gate drivers would be 1.2 W, which is calculated by using (1) with four IRF6691 SRs in the rectifier. Therefore, if the core loss of the inductors is neglected, the proposed gate driver recovers 51% of the gate energy. Given the small inductance, air core inductors can be used, so the core loss would be zero. The total power saving is 0.61 W for the given application, which represents 2% of the total load power, which is significant in view of the high operating efficiencies of present-day converters.

It is also noted that the results given are for a 5-V gate-drive voltage. Because many converters operate with 8–12-V gate-drive voltage, gate loss can be several watts. In this case, the gate energy recovery is even larger. This benefit can be observed from (11), where the dominant first and third terms are inversely proportional to $V_{\rm CC}$ and can be observed later in Section VII where the energy recovery at 12 V improves to above 60% in comparison to 51% at 5-V gate-drive voltage.

VII. IMPACT OF R_G AND PRACTICAL ISSUES

A. Impact of R_G

One of the greatest sources of loss is due to the power-MOSFET internal gate resistance R_G. Because power MOSFETs use a poly gate material, the gate resistance is high. The impact of R_G on gate energy recovery is shown in Fig. 12 at 5-V gate-drive voltage using the circuit parameters from Section VI. In addition, a curve has been provided for 12-V gate-drive voltage. It is clear that as R_G increases, gate energy recovery decreases linearly. The design-example operating point, with 51% energy recovery, is noted in the figure. $R_G = 0.3\ \Omega$ because two IRF6691 MOSFETs have 0.6-Ω R_G each in parallel.

In the RF field, metal-gate connections are often used to minimize gate loss. If this technology is adopted for power

$$L_R = \frac{V_{\rm CC}}{Q_G}\left(\frac{F}{2f_S}\right)^2 \left(\frac{(R_a+R_c)^{2/3}+\left(4R_b+R_c-R_a+2\sqrt{-R_cR_a+4R_b^2+2R_bR_c-2R_bR_a}\right)^{2/3}}{(R_a+R_c)^{1/3}\left(4R_b+R_c-R_a+2\sqrt{-R_cR_a+4R_b^2+2R_bR_c-2R_bR_a}\right)^{1/3}}\right) \tag{13}$$

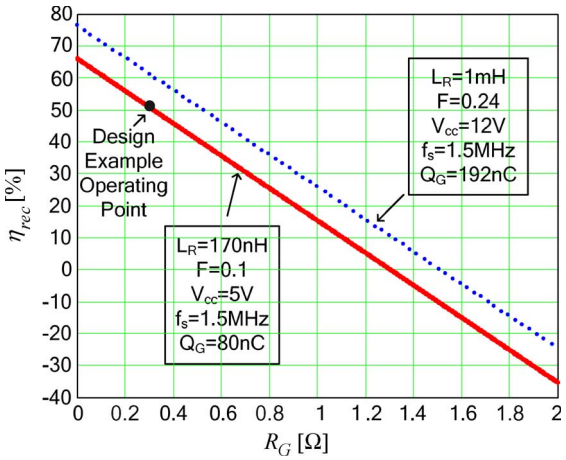

Fig. 12. Gate energy recovery as a function of power-MOSFET gate resistance.

MOSFETs, the energy savings of the proposed driver will improve significantly.

B. Inductor and Timing Tolerances

One of the benefits of the proposed driver is that it behaves like a conventional driver with extra dead time so that the power-MOSFET gate is clamped high or low by the driver switches. This complementary behavior of the control switches makes the driver very robust.

One common issue in implementation is inductor tolerance. In the proposed driver, if the inductor is undersized, the power-MOSFET gate will charge and discharge quicker than expected. If the gate voltage reaches the supply rails during the dead time between Q_1 and Q_3, then the body diodes of Q_1 and Q_3 clamp the voltage high at turn on and low at turn off.

Similarly, if the driver delay times are not optimized, the complementary nature of the control for Q_1 and Q_3 will ensure that the driver operates properly. If the precharge interval t_a is too short, the inductor will not be able to supply sufficient energy during $t_{\rm on}$; however, the remaining energy will be supplied to the gate immediately when Q_1 is turned on. If t_a is too long, the inductor will charge the power-MOSFET gate to $V_{\rm CC}$ quickly during $t_{\rm on}$, and the remaining inductor energy will be sent to the supply voltage using the clamping characteristics of the body diode of Q_1. If the turn-on time $t_{\rm on}$ (t_b) is too short, the remaining gate charge is supplied immediately when Q_1 is turned on. If $t_{\rm on}$ is too long, the gate voltage of Q is clamped to the supply by the body diode of Q_1. If t_c is too short, the excess inductor current returns to the supply through the body diodes of Q_4 and Q_1. If t_c is too long, a small negative current will build up in the inductor, but it is returned to the supply voltage when Q_4 turns off and Q_2 turns on.

C. Range of Duty Cycle Operation

Due to the nearly complementary control of the driver switches Q_1 and Q_3, the proposed driver can operate over a wide range of duty cycles from 0% on the low end to 100% on the high end. The only precaution that needs to be taken

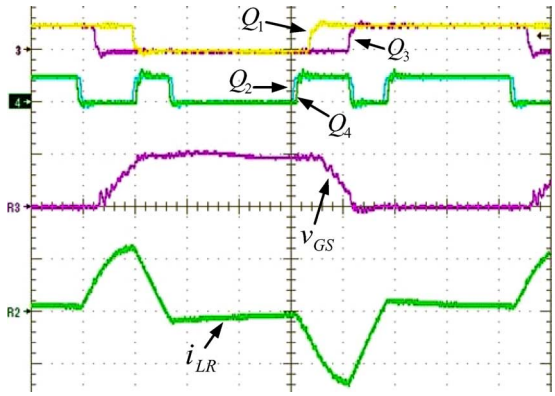

Fig. 13. Key waveforms of the proposed driver used at 1.5-MHz switching frequency. [First (top)] Q_1 and Q_3 gating signals (10 V/div and 80 ns/div). (Second) Q_2 and Q_4 gating signals (10 V/div). (Third) Power-MOSFET gate voltage (5 V/div). [Fourth (bottom)] Inductor current (1 A/div).

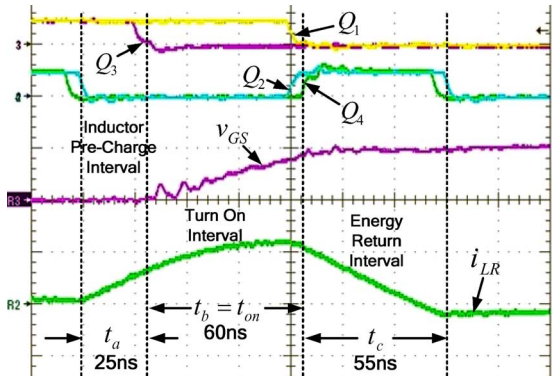

Fig. 14. Key waveforms of the proposed driver used, illustrating the turn-on details at 1.5-MHz switching frequency. [First (top)] Q_1 and Q_3 gating signals (10 V/div and 20 ns/div). (Second) Q_2 and Q_4 gating signals (10 V/div). (Third) Power-MOSFET gate voltage (5 V/div). [Fourth (bottom)] Inductor current (1 A/div).

to mitigate problems with extreme duty-cycle operation is to ensure that Q_2 and Q_4 do not conduct simultaneously, which can be accomplished with simple logic.

VIII. Experimental Results

The proposed driver was built and tested using the same parameters that were given in the design example. The key waveforms are shown in Fig. 13. The top two waveforms are the gating signals for Q_1 and Q_3. The second pair of waveforms is composed of gating waveforms for Q_2 and Q_4. It is noted that there is about 5 ns of dead time between these waveforms. The third waveform is the power-MOSFET gate–source voltage for the two IRF6691 MOSFETs. The bottom waveform is the driver inductor current. The average gate-drive supply current was measured to be 65 mA, which represents a total loss in the circuit of 325 mW, agreeing well with the value of 295 mW calculated in the design example.

Waveforms of the turn-on transition are shown in Fig. 14. The inductor-current precharge time t_a, turn-on time $t_{\rm on}$, and energy return time t_c are clearly evident in the inductor-current waveform. The experimental times of $t_a = 25$ ns, $t_{\rm on} = 60$ ns, and $t_c = 55$ ns agree well with the calculated values of 25, 65,

and 55 ns, respectively. It is noted that the energy return time is about 10 ns long, so the inductor current goes slightly negative as explained in Section VII.

IX. Conclusion

A new resonant gate-drive circuit has been proposed, which solves all three of the problems that are common to existing resonant gate drivers. These problems include the following: 1) high conduction losses during the ON and OFF states of the switch being driven; 2) slow turn-on and turn-off transitions due to the use of an inductance in series with the charging circuit, which begins charging and discharging the gate with zero initial current; and 3) a lack of $Cd\nu/dt$ immunity due to a lack of active clamping at the gate of the device being driven. Furthermore, the inductor used in the proposed method is quite small and is typically approximately 10% of the size of the inductor required in [1].

The logic circuit required to generate the control-switch gating signals has also been presented. A simple design procedure has been included in this section in order to determine the optimum inductor value and delay times. A loss analysis, a design example, and experimental results have been presented. The experimental waveforms agree with the theory, and good agreement was achieved between the loss-analysis calculations (295-mW driver loss) and the experimental results (325-mW driver loss).

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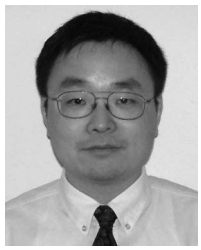

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