High Performance Digital Control Algorithms for DC-DC Converters Based on the Principle of Capacitor Charge Balance

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Abstract— In this paper, the principle of capacitor charge balance is utilized to develop high dynamic performance control algorithms for DC-DC converters. Two digital control algorithms are presented which are designed to drive DC-DC converters, (under load current variation or input voltage variation) to their steady-state conditions in optimum time. The proposed algorithms effectively improve the dynamic response of the converter by reducing the output voltage under/overshoot and minimizing the recovery time. The algorithms' key concepts and equations are presented in this paper. Experimental results are presented for a 25 Watt, 400 kHz synchronous Buck converter to verify the effectiveness of both algorithms. The results confirm that the dynamic response of a DC-DC converter is significantly improved (over that of conventional controllers) by implementing the proposed control algorithms.

I. INTRODUCTION

As the voltage regulation criteria for digital circuits becomes more stringent, there has been an increasing demand for high dynamic performance power converters. Among the many characteristics of dynamic performance, output voltage overshoot/undershoot and recovery time are often considered the most important. In general, the output voltage deviates under load current change, or input voltage change. In order to improve the dynamic response of a DC-DC converter, the switching frequency and/or output filter can be altered. However, this method will result in either an increase in component cost or a decrease in efficiency. By improving the controller dynamic response, the transient performance of a power converter can be improved without topology modification, thereby greatly reducing the component size and cost for high-performance converters.

Numerous control strategies [1]-[5], in analog implementation, have been introduced to provide improved dynamic performance. Transient response is improved in [1] by utilizing load current feed-forward compensation. Unfortunately, this method requires a current transformer in series with the load. This may not be feasible under high output current conditions as it would present a significant voltage drop across the transformer.

Hysteretic current mode controllers provide fast dynamic response since the conventional feedback compensation network is removed; however, this method may not be suitable in many applications due to its variable switching frequency and non-zero steady-state error, as reported in [2].

In [3]-[5], various forms of hysteretic control, based on output voltage ripple, are presented. While these methods improve dynamic performance over conventional linear controllers, they all possess at least one of the following undesired attributes: 1) Variable switching frequency, 2) Non-zero steady-state error, 3) Operating frequencies largely dependant on the equivalent series resistance (ESR) of the output capacitor, (which has large tolerance and can vary significantly with age).

In general, all forms of analog control suffer from at least one of the following conditions: 1) Large component count for complex control methods, 2) Vulnerability to noise, thermal conditions, component age and tolerance, 3) Tedious parameter modification procedures. Most importantly, it is impossible for any of the aforementioned analog controllers to achieve optimal dynamic response (minimal undershoot/overshoot with shortest possible settling time), as it requires complex derivation and calculation, that can only be practically derived digitally.

Compared to analog control, digital control offers many advantages such as re-programmability, reliability and simplicity of complex arithmetic. While extensive research has been conducted in digital controllers that mimic their analog counterparts [6]-[7], a relatively low amount of investigation has been conducted into new digital controller concepts that fully utilize the mathematical capabilities of such systems. In the past, only simple digital PID controllers have been utilized. These control systems suffer from the limitations of slow compensator networks which cause the dynamic performance of the converter to be below satisfactory.

It is demonstrated in [8]-[9], that by implementing two separate control strategies for steady-state and transient conditions, the overall performance of the converter is improved. In [8], two separate sets of linear PID compensators are implemented digitally to provide larger

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bandwidth during transient conditions. While transient response is improved in [8], the controller is still subject to the limitations of slow compensator networks. In [9], a method combining linear voltage mode control and non-linear hysteretic control is introduced. While this method does improve dynamic response, the controller tends to "over-compensate" for load current variations, causing the output voltage to over-shoot after it recovers from a voltage drop, thereby resulting in large settling times.

In this paper, a pair of novel digital control algorithms are introduced that fully-utilize the advanced mathematical capabilities of digital controllers in order to optimize the large-signal response to a load current change and an input voltage change. The digital control algorithms exploit the principle of capacitor charge balance in order to allow the converter to recover in the shortest achievable time with the lowest possible voltage undershoot/overshoot. Implementing the two proposed algorithms together in combination with a conventional digital control scheme will yield a superior large-signal dynamic response with stable steady-state. The proposed algorithms are well-suited to be implemented digitally either using a field programmable gate array (FPGA) or a low-cost application specific integrated circuit (ASIC).

While this paper presents algorithms related solely to the Buck converter, the concept of using capacitor charge balance to optimize dynamic response can be extended to various DC-DC converters including Boost, Buck-Boost and isolated converters.

II. THE PRINCIPLE OF CAPACITOR CHARGE BALANCE

Fig. 1 illustrates a Buck converter.

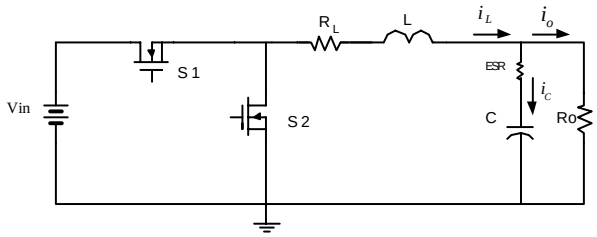

Figure 1: Synchronous Buck Converter

The principle of capacitor charge balance has been utilized extensively for the purpose of steady-state modeling and analysis of DC-DC converters. The principle of capacitor charge balance states that, in steady state, the average of the capacitor current over one switching period must be equal to zero. This condition must be satisfied in order for the output voltage to be equal at the beginning and end of a switching cycle. Equation (1) represents the principle of capacitor charge balance of a Buck converter under steady state.

$$v_c(T_s) - v_c(0) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{T_s}\int_0^{T_s} i_c(t)dt = 0 \qquad (1)$$

By recognizing that the integral period of (1) may be extended over the total transient time of a DC-DC converter, equation (2) is developed.

$$v_c(t_b) - v_c(t_a) = \tfrac{1}{C} \cdot i_{c\,avg} = 0 \rightarrow \frac{1}{t_b - t_a}\int_{t_a}^{t_b} i_c(t)dt = 0 \qquad (2)$$

where t_a represents the beginning of the transient period and t_b represents the end of the transient period. Thus, if at t_b the inductor current i_L and the duty d have reached their new steady state values, and (2) has been satisfied, the converter will immediately enter its new steady state without any switchover.

The proposed pair of control algorithms exploits the aforementioned concept in order to minimize the recovery time t_b-t_a and voltage under/overshoot under transient conditions.

In contrast, figure 2 demonstrates a typical transient response to a load current change under voltage mode control (or any other analog control method). As observed, at point 3, although the output voltage has recovered to the reference voltage, the converter is still in transient state. The inductor current must decrease toward the new load current. When the inductor current is equal to the load current at point 4, the charge delivered to the capacitor A_{charge} is greater than the charge removed from the capacitor $A_{discharge,}$ therefore the voltage has not recovered to its steady state value. The converter will continue this behavior in a cyclical pattern for many more switching cycles before it settles and reaches steady state.

Therefore, for conventional controllers, the recovery time is long and the voltage deviation is large.

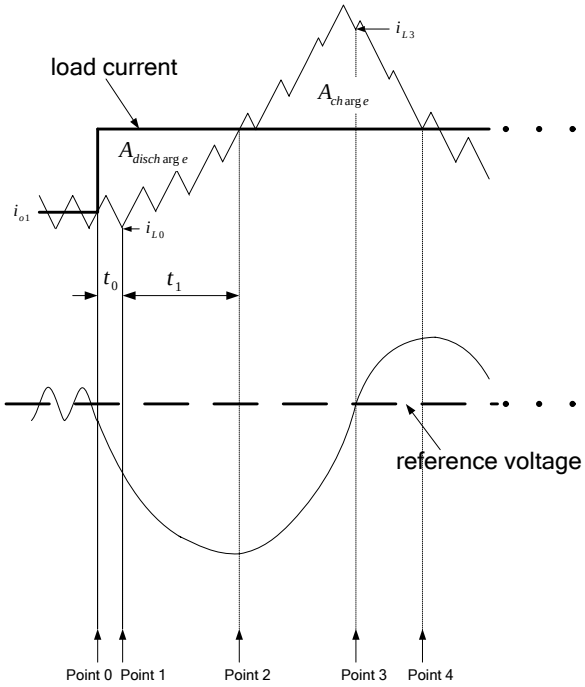

Figure 2: Transient Response of a Buck Converter Under Voltage Mode Control

III. OPTIMAL DYNAMIC RESPONSE UNDER LOAD CURRENT CHANGE

The proposed algorithm optimizes the dynamic response

of a Buck converter under a load current step change. While the algorithm is valid for both positive and negative load current changes, the analysis and derivation of a positive change will be examined in this paper.

In order for a converter to achieve the best possible dynamic response (lowest undershoot, shortest recovery time) to a load current change, the following observations are made:

1. Following a positive load current step change, the inductor current can not change instantaneously and therefore a portion of the load current is supplied by the output capacitor. This in turn causes the capacitor voltage and the output voltage to reduce. In order to minimize the voltage drop, it is necessary for the inductor current to increase at its fastest possible slew rate. Therefore, the duty cycle must be at its maximum.
2. The capacitor voltage will be at its minimum at the moment the inductor current reaches the level of the output current. The inductor current will continue to rise, causing the capacitor to charge and the output voltage to increase.
3. At a specific point (to be determined), the duty cycle should be set to its minimum, to drive the inductor current toward its new steady state value.
4. In order to achieve the minimum possible settling time, the charge delivered to the capacitor must be equal to the charge previously removed from the capacitor at the exact moment that the inductor current reaches its new steady state value. This is the primary objective of the algorithm.

The algorithm is based on the aforementioned principles. Fig. 3 illustrates the algorithm's response to a positive load current step change. The load current step change occurs at point 0. At point 1, the large voltage deviation is sensed by the controller and the system switches from the conventional steady-state controller (in this case, a digital current-mode PID controller) to the proposed large-signal algorithm. The duty cycle is set to 100% for the time period t_{up} in order to ramp up the inductor current. The duty cycle is then set to 0% for the time period t_{down}, to drive the inductor current toward its new steady-state value. At Point 5, the inductor current reaches its new steady-state value and the system returns to the steady-state controller. In order to guarantee that the converter is fully recovered at point 5, the principle of capacitor charge balance must hold at this point (i.e. (3) must be satisfied).

$$A_0 + A_1 + A_3 = A_2 \tag{3}$$

There are six key steps to the proposed algorithm. The following derivation applies to a positive load step; however, the derivation for a negative load step is virtually identical.

Step 1: Estimate new load current (i_{o2})

For large output currents, it is difficult to sense the load current directly without creating a large voltage drop at the output. Thus, the algorithm indirectly estimates the new load current by sensing the output voltage response.

To estimate the new load current value, the output voltage, v_{o1}, the inductor current i_{L1} at point 1, the output voltage, v_{oa}, and the inductor current, i_{La} at point 1.a are sensed. The time period between these two sample points, t_{1a}, is known. During the time interval, t_{1a}, the change of output capacitor charge can be written as (4), and re-written as (5).

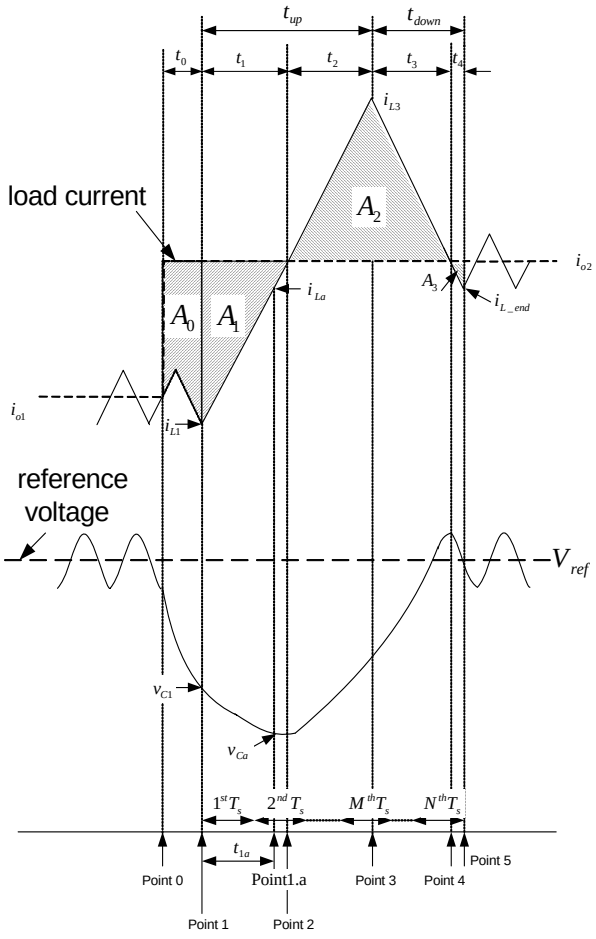

Figure 3: Dynamic response of Buck converter under positive current step change with proposed algorithm

$$C\Delta v_C = C(\Delta v_0 - \Delta i_C ESR) \tag{4}$$

$$\begin{aligned} C \cdot \Delta v_C &= C \cdot [(v_{0a} - v_{o1}) - (i_{Ca} - i_{C1}) \cdot ESR] \\ &= \int_{po\ int\ 1}^{po\ int\ 1.a} (i_L - i_{o2}) \cdot dt \end{aligned} \tag{5}$$

In (5), i_{Ca} and i_{C1} are the capacitor currents at point 1.a and point 1 respectively. Since i_{C1}=i_{L1}-i_{o2}, i_{Ca}=i_{La}-i_{o2}, and i_{C2}-i_{C1}=i_{La}-i_{L1}, (5) can be approximated in discrete-time form in (6).

$$C \cdot (v_{0a} - v_{o1}) = \frac{1}{2}(i_{L1} + i_{La}) \cdot t_{1a} - i_{o2} \cdot t_{1a} + (i_{La} - i_{L1}) \cdot C \cdot ESR \tag{6}$$

Isolating i_{o2}, the load current can be estimated using (7).

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{La}) - \frac{C \cdot (v_{0a} - v_{o1}) - C \cdot (i_{La} - i_{L1}) \cdot ESR}{t_{1a}} \tag{7}$$

Step 2: Calculate inductor slew rates

The rising and falling slew rates for the inductor current of a Buck converter are expressed in equations (8) and (9) respectively.

$$\frac{di_L}{dt} = \frac{v_{in} - v_o'}{L} \tag{8}$$

$$\frac{di_L}{dt} = \frac{-v_o'}{L} \tag{9}$$

v_o' is approximated in (10).

$$v_o' \approx V_{ref} + i_{o2} \cdot r_{loss} \tag{10}$$

r_{loss} represents the equivalent loss of the converter and is expressed in (11).

$$r_{loss} = R_L + R_{on} + R_{switching} \tag{11}$$

R_L is the inductor resistance, R_{on} is the MOSFET resistance and $R_{switching}$ represents the equivalent switching loss.

Step 3: Calculate the capacitor discharge portion A_0

A_0 can be estimated using (12).

$$\begin{aligned} A_0 &= C \cdot (v_{C0} - v_{C1}) \approx C \cdot (V_{ref} - v_{C1}) = C \cdot (V_{ref} - v_{o1} + i_{C1} \cdot ESR) \\ &= C \cdot (V_{ref} - v_{o1} + (i_{L1} - i_{o2}) \cdot ESR) \end{aligned} \tag{12}$$

Step 4: Calculate t_1 and the capacitor discharge portion A_1

Based on the estimated load current i_{o2} and the inductor current rising slew rate given by (8), the interval t_1 and the capacitor discharge A_1 can be obtained utilizing simple geometry, as defined in (13) and (14).

$$t_1 = \frac{i_{o2} - i_{L1}}{(v_{in} - v_o')/L} \tag{13}$$

$$A_1 = \frac{1}{2} t_1 (i_{02} - i_{L1}) \tag{14}$$

Step 5: Calculate t_4 and the capacitor discharge portion A_3

When the transient ends, the new steady state duty cycle is obtained using (15).

$$D_{new} = \frac{v_o'}{v_{in}} \tag{15}$$

The value of the new steady state inductor current ripple can be expressed as (16).

$$I_{ripple} = (1 - D_{new}) \cdot T_s \cdot \frac{v_o'}{L} \tag{16}$$

Therefore, the new steady state inductor current valley value i_{L_end} is given by (17).

$$i_{L\_end} = i_{o2} - \frac{1}{2} I_{ripple} = i_{o2} - \frac{1}{2}(1 - \frac{v_o'}{v_{in}}) \cdot T_s \cdot \frac{v_o'}{L} \tag{17}$$

Based on the estimated load current, i_{o2}, the inductor current falling slew rate, given by (9), and the new steady state inductor current valley value, given by (17), the interval t_4 and the capacitor discharge area, A_3 can be obtained geometrically using (18) and (19).

$$t_4 = \frac{i_{o2} - i_{L\_end}}{v_o'/L} \tag{18}$$

$$A_3 = \frac{1}{2} t_4 \cdot (i_{02} - i_{L\_end}) \tag{19}$$

Step 6: Calculate the capacitor charge A_2 and the time periods t_2 and t_3

It is noted in Fig. 3 that at point 5, the charge removed from the capacitor is equal to the charge delivered to the capacitor, thus (3) is satisfied.

During the time period t_2, the inductor current slew rate is given by (8). During the time period t_3, the inductor current slew rate is given by (9). Therefore, the capacitor charge area A_2 can be derived geometrically in (20), where i_{L3} is given by (21) .

$$A_2 = \frac{1}{2}(t_2 + t_3) \cdot (i_{L3} - i_{02}) \tag{20}$$

$$i_{L3} = i_{o2} + \frac{v_0'}{L} \cdot t_3 = i_{o2} + \frac{v_{in} - v_0'}{L} \cdot t_2 \tag{21}$$

Using (21), the ratio t_2/t_3 can be derived as (22).

$$t_2 / t_3 = \frac{v_o'}{v_{in} - v_o'} \tag{22}$$

Then, using (12), (14), (19) and (20)–(22), the times t_2 and t_3 can be derived as (23) and (24).

$$t_2 = \sqrt{\frac{A_0 + A_1 + A_3}{\frac{1}{2}\frac{v_{in}}{v_o'}\frac{v_{in} - v_o'}{L}}} \tag{23}$$

$$t_3 = \frac{v_{in} - v_o'}{v_o'} t_2 \tag{24}$$

In order to achieve optimal dynamic response, the rise time $t_{up} = t_1 + t_2$ and the fall time $t_{down} = t_3 + t_4$ is calculated.

The controller uses the calculated times to drive the converter to recover in the shortest possible time. Since the duty cycles of the converter can only be altered at discrete times, the algorithm compensates for this by adjusting two duty cycles during the transient period.

Before the converter returns to its steady-state mode, the algorithm passes the new duty cycle (15) and load current (7) to the digitally-implemented current-mode PID controller.

IV. OPTIMAL DYNAMIC RESPONSE UNDER INPUT VOLTAGE CHANGE

The principle of capacitor charge balance can be applied to ensure that a converter, under an input voltage change, can recover in optimal time. An algorithm is proposed to drive a converter to recovery in two switching cycles after an input voltage change.

While analog current-mode controllers may have excellent audio-susceptibility, digital current-mode controllers do not. Therefore, this algorithm corrects a major drawback of digitally-implemented controllers.

Fig. 4 illustrates the dynamic response of the proposed

algorithm when the input voltage changes within one switching cycle. The following analysis and derivation will pertain to a positive input voltage step; however, the derivation of a negative input voltage step is virtually identical.

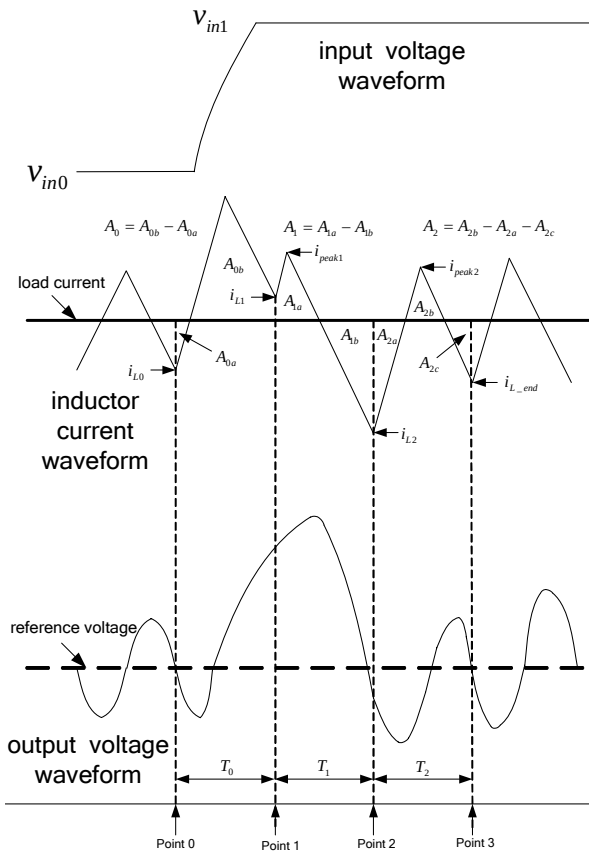

Figure 4: Dynamic Response of proposed algorithm under positive input voltage change

As with the previous algorithm, the main goal of the input voltage algorithm is to ensure that the principle of capacitor charge balance is satisfied at the exact moment that the inductor current reaches its steady-state value, after the transient. At point 3, it is apparent that the inductor current is at its steady state value. In order for the converter to be considered recovered, the charge removed from the capacitor must equal the charge delivered to the capacitor.

The input voltage variation is sensed directly by the controller. The system will switch from its conventional steady-state controller to the proposed algorithm immediately following an input voltage variation.

As with the previous algorithm, the first step of derivation is to determine the capacitor charge portion A_0. A_0 represents the capacitor charge change before the algorithm senses the voltage variation and activates. A_0 is calculated in (25).

$$\begin{aligned} A_0 &= C \cdot (v_{C1} - v_{C0}) \approx C \cdot (v_{C1} - V_{ref}) \\ &= C \cdot (v_{o1} - i_{C1} \cdot ESR - V_{ref}) \\ &= C \cdot (v_{o1} - (i_{L1} - i_o) \cdot ESR - V_{ref}) \end{aligned} \tag{25}$$

A_1 represents the net capacitor charge during period T_1. A_1 is calculated geometrically in (26).

$$\begin{aligned} A_1 &= \frac{1}{2} d_1 T_s \cdot \left[(i_{L1} - i_{L2}) + (i_{peak1} - i_{L2}) \right] \\ &+ \frac{1}{2} (1 - d_1) T_s \cdot (i_{peak1} - i_{L2}) - (i_o - i_{L2}) T_S \end{aligned} \tag{26}$$

where d_1 represents the duty cycle of period T_1.

A_2 represents the net capacitor charge during the period T_2. A_2 is calculated geometrically in (27).

$$\begin{aligned} A_2 &= \frac{1}{2} d_2 T_s \cdot (i_{peak2} - i_{L2}) \\ &+ \frac{1}{2} (1 - d_2) T_s \cdot \left[(i_{peak2} - i_{L2}) + (i_{L\_end} - i_{L2}) \right] \\ &- (i_o - i_{L2}) T_S \end{aligned} \tag{27}$$

where d_2 represents the duty cycle of period T_2.

In order to ensure that the converter is recovered at point 3, the inductor current must equal its steady state value at the exact moment that (28) is satisfied.

$$A_0 + A_1 + A_2 = 0 \tag{28}$$

Referring to Fig. 4, a relationship between i_{L1} and i_{L_end} is established in (29).

$$i_{L\_end} - i_{L1} = (d_1 v_{in1} - v_o') \frac{T_s}{L} + (d_2 v_{in1} - v_o') \frac{T_s}{L} \tag{29}$$

v_o' is previously calculated in (10).

Re-arranging (29) yields a relationship between d_1 and d_2, as expressed in (30).

$$d_1 + d_2 = \frac{(i_{L\_end} - i_{L1}) \cdot \frac{L}{T_s} + 2 \cdot v_o'}{v_{in1}} = k \tag{30}$$

By combining (25)-(28) and (30), the required duty cycles are expressed in (31) and (32).

$$d_1 = \frac{1}{2} \left[(1+k) - \sqrt{(1+k)^2 + \frac{4L}{v_{in1} \cdot T_s} (i_{L1} - 2 i_o + i_{L\_end} - \frac{1}{2} k^2 v_{in1} \frac{T_s}{L} + \frac{A_0}{T_s})} \right] \tag{31}$$

$$d_2 = k - d_1 \tag{32}$$

The algorithm uses the calculated duty cycles to drive the converter to recovery in two switching cycles.

Due to the presence of input filters, input voltage changes are usually slow. The algorithm compensates for slow voltage changes by continuously sensing the input voltage to determine if the input voltage change has completed. In this case, the converter will recover two switching cycles after the input voltage variation ceases.

It is possible, under very large input voltage variations, that (31) and (32) yield duty cycles below 0% or above 100%. In this case, the algorithm will continuously reset and recalculate the duty cycles until feasible results are obtained.

V. Experimental Results

In order to verify the functionality of the algorithms, they were tested using the setup illustrated in Fig. 5.

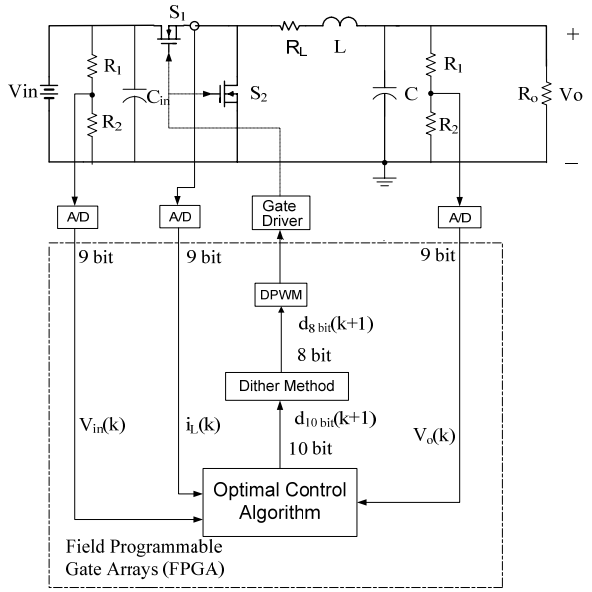

Figure 5: Experimental test setup

The Buck converter under test had the following parameters: 25W, *L*=1uH, *C*=235uF, ESR=1mΩ, R_L=2mΩ and *fs*=400kHz.

An FPGA was utilized in order to implement a digital current-mode PID controller and the two dynamic response algorithms. The FPGA used was a Xilinx Spartan 2E development board with a clock speed of 200 MHz.

The dynamic response of the two algorithms was compared with that of a digitally-implemented current-mode PID controller. The PID controller was designed for maximum bandwidth with a phase margin of 50º.

A. Load Current Step Dynamic Response

The above-mentioned controller was tested with a positive load current step of 5A→10A. The input voltage was set to 5V and the reference voltage was set to 2.5V. Fig. 6 and Fig. 7 illustrate the response of the PID controller and the proposed algorithm respectively.

It is shown in Fig. 6 and Fig. 7 that by using the proposed control algorithm, the voltage undershoot, due to a positive load current step change (5A→10A), is decreased from 132mV using current-mode PID to 86mV using the proposed optimal control algorithm.

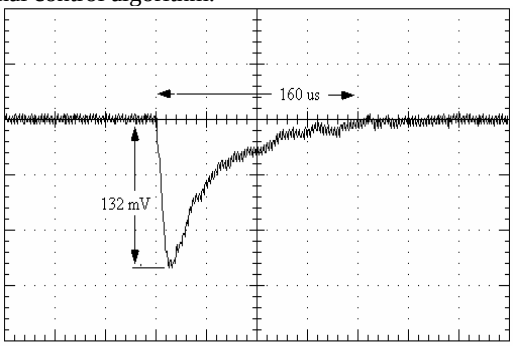

Figure 6: PID controller response to a 5A→ 10A load current step
(X-axis: 40us/div; Y-axis: 50mV/div)

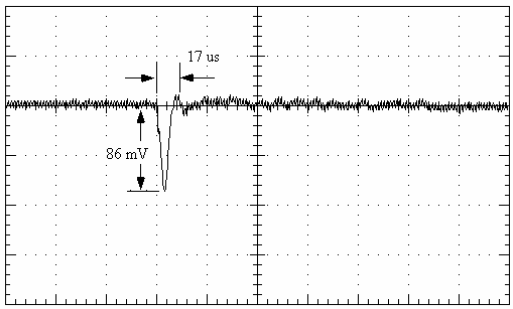

Figure 7: Optimal algorithm response to a 5A→ 10A load current step
(X-axis: 40us/div; Y-axis: 50mV/div)

The recovery time is reduced from 160us using the current-mode PID controller to 17us using the proposed optimal control algorithm.

The converter was tested with a negative load current step of 10A → 5A. Fig. 8 and Fig. 9 illustrate the response of the PID controller and the proposed algorithm respectively.

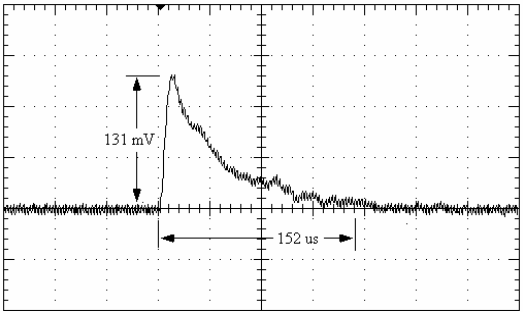

Figure 8: PID controller response to a 10A→ 5A load current step
(X-axis: 40us/div; Y-axis: 50mV/div)

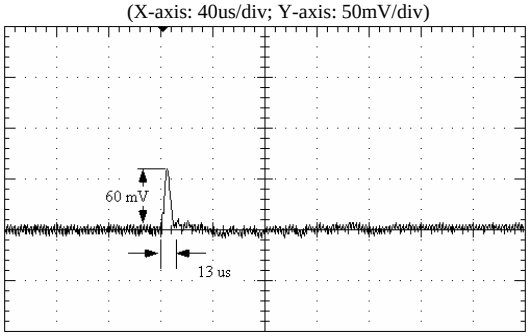

Figure 9: Optimal algorithm response to a 10A→ 5A load current step
(X-axis: 40us/div; Y-axis: 50mV/div)

It is demonstrated in Fig. 8 and Fig. 9 that by using the proposed control algorithm, the voltage overshoot, due to a negative load current step change (10A→5A), is decreased from 131mV using the current mode PID controller to 60mV using the proposed optimal control. The recovery time is reduced from 152us using current-mode PID to 13us using the proposed optimal control algorithm.

B. Input Voltage Change Dynamic Response

The converter was tested with a negative input voltage change of 7.5V → 5V. The output current was set to 5A for this experiment. Fig. 10 and Fig. 11 illustrate the response of the PID controller and the proposed algorithm respectively.

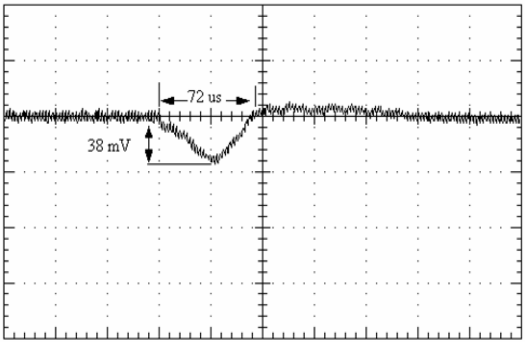

Figure 10: PID controller response to a 7.5V→5V input voltage change (X-axis: 40us/div; Y-axis: 50mV/div)

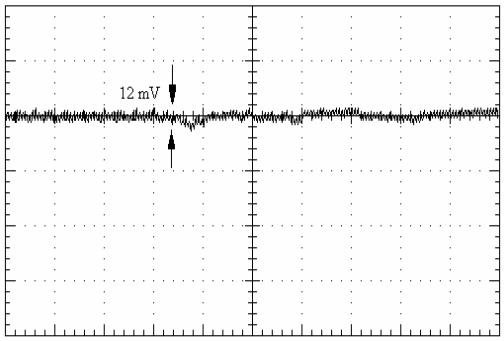

Figure 11: Optimal algorithm response to a 7.5V→5V input voltage change (X-axis: 40us/div; Y-axis: 50mV/div)

It is demonstrated in Fig. 10 and Fig. 11 that by using the proposed control algorithm, the voltage undershoot, due to a negative input voltage change (7.5V→5V), is decreased from 38mV using the current-mode PID controller to 12mV using the proposed optimal control algorithm. The recovery time is reduced from 72us using the current-mode PID controller to 12us using the proposed optimal control algorithm.

Similar improvement is achieved when the input voltage undergoes a positive change from 5V→7.5V.

VI. CONCLUSION

This paper demonstrates how the concept of capacitor charge balance can be utilized to develop digitally-implemented algorithms that significantly improve the dynamic response of DC-DC converters. While, this paper focused on the Buck topology, the principle of capacitor charge balance can be applied to other DC-DC converters in order to develop algorithms to improve their dynamic response.

The pair of algorithms are verified through experimentation. The experimental results demonstrate a significant improvement in dynamic response during a load current variation and during an input voltage variation. Since the algorithms are implemented in conjunction with traditional PID current-mode controllers, the converter can significantly improve large-scale dynamic response performance while maintaining stable steady-state. By focusing on capacitor charge balance, high-performance digital algorithms can be developed for DC-DC converters that far surpass the dynamic response performance of traditional analog control schemes.

VII. REFERENCES

[1] S. Kanemaru, T. Hamada, T. Nabeshima, T. Sato, T. Nakano, "Analysis and optimum design of a buck-type DC-to-DC converter employing load current feedforward", IEEE 35th Annual Power Electronics Specialists Conference (PESC 98), Vol. 1 pp. 309 – 314

[2] C. Song; J.L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator", IEEE 20th Annual Applied Power Electronics Conference and Exposition (APEC 05) IEEE, Vol. 1 pp. 276 – 280

[3] R. Miftakhutdinov, "Optimal design of interleaved synchronous buck converter at high slew-rate load current transients" IEEE 32nd Annual Power Electronics Specialists Conference (PESC 01), Vol. 3 pp. 1714 – 1718

[4] J. Zhao, T. Sato, T. Nabeshima, T. Nakano, "Steady-state and dynamic analysis of a buck converter using a hysteretic PWM control", IEEE 35th Power Electronics Specialists Conference (PESC 04), Vol. 5 pp. 3654 – 3658

[5] J. Zhao, T. Sato, T. Nabeshima, T. Nakano, "A new PWM control scheme using a triangle waveform modulated by output voltage", IEEE 19th Applied Power Electronics Conference and Exposition (APEC 04), Vol. 1 pp. 399 – 403

[6] B.J. Patella, A. Prodic, A. Zirger, D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters", IEEE Transactions on Power Electronics, Vol. 18, No. 1, 2003, pp. 438-446

[7] Y. Duan, H. Jin, "Digital controller design for switchmode power converters", IEEE 14th Annual Applied Power Electronics Conference and Exposition (APEC 99), Vol. 2, pp. 967-973

[8] L. Guo J.Y. Hung, R.M. Nelms, "PID controller modifications to improve steady-state performance of digital controllers for buck and boost converters", IEEE 17th Annual Applied Power Electronics Conference and Exposition, (APEC 02), Vol. 1, pp. 381-388

[9] A. Barrado, J. Quintero, A. Lazaro, C. Fernandez, P. Zumel, E. Olias, "Linear-Non-Linear Control Applied in Multiphase VRM", IEEE 36th Annual Power Electronics Specialists (PESC 05), pp. 904 – 909