A Direct Duty Cycle Calculation Algorithm for Digital Power Factor Correction (PFC) Implementation

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Abstract—A new PFC control method based on direct duty cycle calculation is proposed. The duty cycle required to achieve unity power factor is calculated directly based on the reference current and sensed inductor current, input voltage and output voltage. For both digital and analog implementation, the proposed PFC control method is simpler than commonly used average current mode control. Test results for a digital implementation show that the proposed method can achieve unity power factor under both steady and transient state. Sinusoidal input current can be achieved under non-sinusoidal input voltage condition. The proposed digital PFC control method can achieve good dynamic performance for load and input voltage change.

I. INTRODUCTION

There are several disadvantages in the existing digital control PFC implementation based on conventional current mode control, such as high computation requirement, limited switching frequency and high cost [1][2]. Predictive control methods are being explored and implemented in digital controlled PFC in order to take full advantage of digital techniques. Digital current program control using predictive algorithm was presented in [3]. In that paper, the duty cycle, d(n+1), was calculated based on the value of the present duty cycle d(n) and sensed inductor current, input voltage and output voltage. Unity power factor was achieved. The first disadvantage is that the duty cycle calculation requires the duty cycle value in the previous switching cycle. Second, the computation requirement is not obviously reduced compared to that in the digital PFC implementation based on current mode control. Reference [4] proposed dead-beat predictive control in which a predicted duty cycle was used to control the switch during a control period which is equivalent to several or several tens switching cycles. The duty cycles were fixed during one control period. Computation was reduced in that control method. However, the harmonics in the line current was increased compared to the control method in which the duty cycle was calculated in every switching cycle. The computation requirement in digital PFC implementations was reduced further by the techniques proposed in [5] [6] because all the duty cycles for a half line period were calculated in advance based on the voltage loop and the input voltage feed-forward. However, the current waveform is sensitive to the parameters of the model and the capability of the regulation to the step load change is not satisfied when the load variation is wide.

A direct duty cycle calculation algorithm with only voltage loop regulator for digital power factor correction implementation is proposed in this paper. The proposed control method can achieve unity power factor under both steady and transient state. This PFC control method can be implemented by a low cost DSP due to its low computation requirement. It overcomes the disadvantages of the existing digital PFC techniques mentioned above, such as high computation requirement, model sensitivity and increased harmonics, etc.

II. DIRECT DUTY CYCLE CALCULATION ALGORITHM FOR PFC WITH BOOST TOPOLOGY

Boost topology used in PFC implementation is shown Fig. 1. The proposed digital control PFC algorithm is derived based on the assumptions that the Boost converter operates at continuous conduction mode (CCM) and the switching frequency is much higher than the line frequency (the input voltage, V_{in}, can be assumed as a constant in one switching cycle, T_s). Therefore, when the switch S is on or off, the Boost converter is described as two equivalent circuits, as shown in Fig. 2. Differential equation (1) and (2) describe the inductor current in one switching cycle when switch is on or off, respectively.

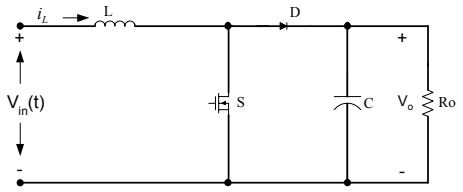
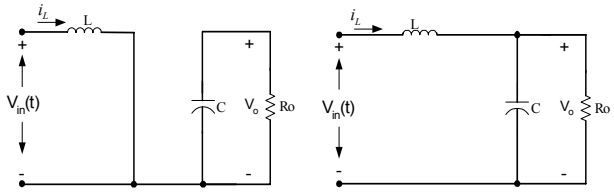


Fig. 1 Boost converter topology



(a) switch is on (b) switch is off

Fig. 2 Boost converter equivalent circuit

$$L\frac{di_L}{dt} = V_{in} \qquad t_n \le t < t_n + d_n T_s \tag{1}$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_n + d_n T_s \le t < t_{n+1} \tag{2}$$

* US and International Patent Pending

Substituting $\frac{di_L}{dt} \approx \frac{i_L(n+\Delta t)-i_L(n)}{\Delta t}$ ($\Delta t \to 0$) into (1) and (2), the inductor current at the end of one switching cycle can be expressed as

$$i_L(n+1) = i_L(n) + \frac{V_{in}(n)\cdot T_s}{L} - \frac{V_o(1-d(n))\cdot T_s}{L} \quad (3)$$

Equation (3) can be rearranged as:

$$d(n) = \frac{L}{T_s}\frac{i_L(n+1)-i_L(n)}{V_o} + \frac{V_o - V_{in}(n)}{V_o} \quad (4)$$

It is observed from (4) that the duty cycle in each switching cycle could be determined properly to achieve unity power factor. In a properly designed AC-to-DC converter with PFC, $i_L(n+1)$ is forced to follow the reference current, $i_{ref}(n+1)$, which is a rectified sinusoidal waveform, as shown in Fig. 3. V_o is controlled to follow the reference voltage, V_{ref}. Substituting $i_{ref}(n+1)$, V_{ref} for $i_L(n+1)$ and V_o in (4), the duty cycle can be derived as

$$d(n) = \frac{L}{T_s}\frac{i_{ref}(n+1)-i_L(n)}{V_{ref}} + \frac{V_{ref} - V_{in}(n)}{V_{ref}} \quad (5)$$

where $i_L(n)$ is the sensed current. The duty cycle calculated by (5) can achieve unity power factor in Boost converter.

There are two components in (5), expressed as

$$d(n) = d_1(n) + d_2(n) \quad (6)$$

The first component, $d_1(n)$, expressed as

$$d_1(n) = \frac{(i_{ref}(n+1)-i_L(n))\cdot\frac{L}{T_s}}{V_{ref}} \quad (7)$$

is defined as Current Forcing Component (CFC). In steady state, the inductor current, $i_L(n+1)$, follows the reference current, $i_{ref}(n+1)$, at the end of that switching cycle. Therefore, the numerator of (7) is actually the inductor current differentiation in one switching cycle: $V_L(t) = L\frac{di_L(t)}{dt} \approx \frac{L}{T_s}[i_L(n+1)-i_L(n)]$. In transient state, $d_1(n)$ force the inductor current follow the reference current which is determined by the power balance between the input and output of the converter. $d_1(n)$ guarantees the output voltage, V_o, be regulated to follow the reference voltage for transient state.

In (7), the reference current is determined as

$$i_{ref}(n+1) = k_{PID}\cdot\left|\sin(\omega_{line}\cdot t(n+1))\right| \quad (8)$$

k_{PID} is the peak value of the reference current, which is the output of the voltage loop controller. $|sin(\omega_{line}\cdot t(n)|$ is the rectified line frequency sinusoidal waveform, which is stored as a look up table, as shown in Fig. 5. In the implementation, the input voltage could be sensed and processed to produce the unity rectified line frequency sinusoidal waveform. The advantage of using the look up table to generate $|sin(\omega_{line}\cdot t(n)|$ is that the sinusoidal input current waveform can be achieved under non-sinusoidal input voltage condition. This is verified by the experimental results in section V.

The second component, $d_2(n)$, expressed as

$$d_2(n) = 1 - \frac{V_{in}(n)}{V_{ref}} \quad (9)$$

is determined by the input and output voltage equilibrium of Boost topology. Therefore, d_2 is defined as Voltage Equilibrium Component (VEC). In (9), $V_{in}(n)$ is the instantaneous input voltage value sensed by the input voltage fed-forward channel, as shown in Fig. 5. $d_2(n)$ can guarantee V_o be stable for input voltage variation.

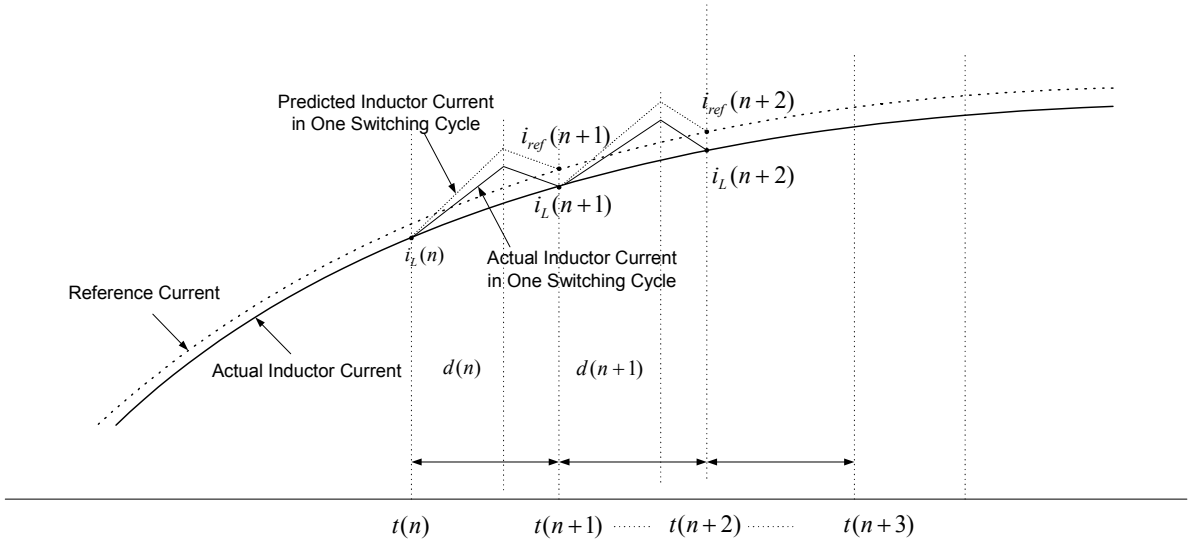


Fig. 3 Inductor current controlled by the directly calculated duty cycles

Substitute (8) into (5), the proposed PFC control algorithm can be expressed as:

$$d(n) = \frac{k_{PID} \cdot \left|\sin(\omega_{line} \cdot t(n+1)\right| - i_L(n)}{K_c} + \frac{V_{ref} - V_{in}(n)}{V_{ref}} \qquad (10)$$

where, $K_c = T_s \cdot V_{ref} / L$, is a constant which characterizes the inductor current variation in one switching cycle when only the reference voltage is applied on the inductor. This constant is defined as Intrinsic Current Slope Constant in this paper. It can be used to simplify the proposed PFC control algorithm in the implementation.

The duty cycle in (5), *d(n)*, is generated based on: (1) the actual inductor current, $i_L(n)$, which is sensed at the beginning of the present switching cycle *t(n),* and (2) the desired inductor current, $i_{ref}(n+1)$, which is the reference current value at the beginning of the next switching cycle, *t(n+1),* as shown in Fig. 3. The inductor current is controlled by *d(n)* to follow the reference current. At *t(n+1),* the inductor current $i_L(n+1)$ may not be exactly the same as, but very close to the reference current $i_{ref}(n+1)$. Because the reference current is sinusoidal, the actual inductor current will also be sinusoidal to achieve unity power factor.

2.1 Simplification of the Proposed PFC Control Algorithm

In the digital implementation of the proposed duty cycle calculation algorithm, (6), (7) and (9) can be simplified by multiplying all the parameters with the Constant K_c, as:

$$D(n) = D_1(n) + D_2(n) \qquad (11)$$

$$D_1(n) = k_{pid} \cdot |\sin(\omega_{line} \cdot t(n+1))| - i_L(n) \qquad (12)$$

$$D_2(n) = K_c - V_{in}^{'}(n) \qquad (13)$$

where, $D_1(n) = d_1(n) \cdot K_c$, $D_2(n) = d_2(n) \cdot K_c$, $V_{in}^{'}(n) = \frac{V_{in}(n)}{V_{ref}} \cdot K_c = \frac{T_s}{L} V_{in}(n)$. *D(n), $D_1(n)$* and *$D_2(n)$* are simplified values of duty cycle, *d(n),* and its components, $d_1(n)$ and $d_2(n)$.

It is observed from (11), (12) and (13) that after simplification, only one multiplication and three additions (subtractions) are required in order to implement the proposed duty cycle control algorithm. Therefore the digital implementation of the proposed PFC control algorithm is very simple. A low cost DSP, microprocessor, FPGA or an ASIC can be used to implement PFC operating at high switching frequency because of its low computation requirement.

III. ANALOG IMPLEMENTATION

It is easy to convert (10) from discrete form back to continuous form, as:

$$d(t) = \frac{k_{PID} \cdot \left|\sin(\omega_{line} \cdot t)\right| - i_L(t)}{K_c} + \frac{V_{ref} - V_{in}(t)}{V_{ref}} \qquad (14)$$

where $i_L(t)$ is the average value of the inductor current.

Corresponding to (11), (12) and (13), the simplified continuous form of the proposed direct duty cycle control algorithm can be expressed as:

$$D(t) = D_1(t) + D_2(t) \qquad (15)$$

$$D_1(t) = k_{pid} \cdot |\sin(\omega_{line} \cdot t)| - i_L(t) \qquad (16)$$

$$D_2(t) = K_c - V_{in}^{'}(t) \qquad (17)$$

Hence, based on (15), (16) and (17), the proposed direct duty cycle control method could be easily implemented by analog control, as shown in Fig. 4. Again, only one multiplier and three adders are required for the implementation. Therefore, for analog implementation, the proposed PFC control method is simpler than commonly used average current mode control for PFC implementation.

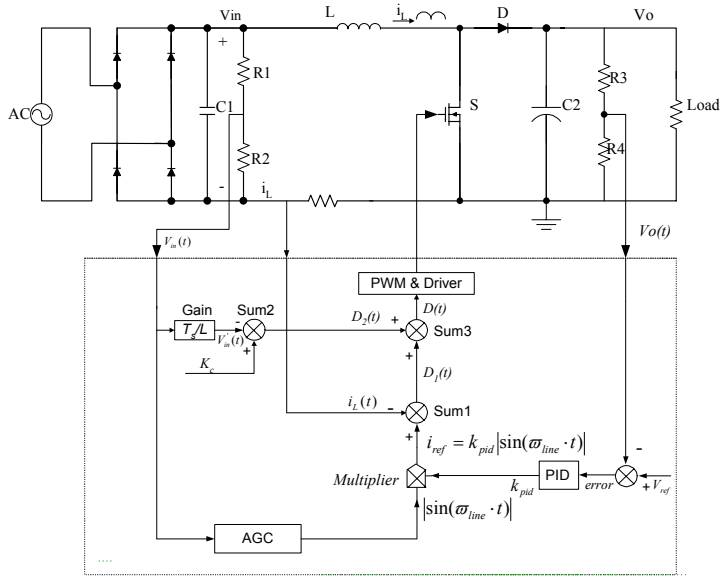


Fig. 4 Analog implementation of the proposed PFC control method

In Fig. 4, an automatic gain control module (AGC) is used to convert the sensed input voltage to a unity rectified sinusoidal waveform to eliminate the effect due to the variation in the input voltage. The output of the voltage regulation multiplies the unity rectified sinusoidal waveform to produce the reference current. Sum1 in Fig. 4 is used to perform (16) which determines the duty cycle component $D_1(t)$ based on the $i_{ref}(t)$ and $i_L(t)$. Sum2 is used to perform (17) which determines the duty cycle component $D_2(t)$ based on the constant K_c and $V_{in}^{'}(t)$. $V_{in}^{'}(t)$ is obtained from V_{in} by the scaling factor T_s/L. Sum3 is used to perform (15) which determines the duty cycle for the switch. PWM and driver block is used to convert the voltage signal to actual duty cycle to drive the MOSFET in Boost converter.

IV. DSP IMPLEMENTATION

The DSP implementation diagram of the proposed digital PFC control method is shown in Fig. 5. The output voltage is sensed and fedback to the DSP via 10bit A/D converter. The feedback output voltage signal is compared with the reference voltage and the difference produces the error signal for the voltage regulator. The output of voltage regulator determines the amplitude of the reference current. The input voltage is sensed for the zero crossing signal detection and input voltage fed-forward. The gate signal is determined by the duty cycle calculation and provided for the switch via the PWM module of DSP. A Boost circuit controlled by a DSP evaluation board is shown in Fig. 6.

In the hardware implementation, the main component values of the Boost circuit are: $L=1.2mH$, output filter capacitor $C=1100uF$. The test operating parameters are chosen as: rated input voltage $V_{in}=110V(RMS)$, output power $P_{load}=600W$(full load current $I_o=3A$), output voltage $V_{out}=200V$, switching frequency $f_{sw}=160kHz$ and line frequency $f_{line}=50Hz$. $1.2mH$ inductor used in the implementation is for the purpose of reducing the ripple current. In practical design, smaller inductor can be used.

In practical implementation, soft-start and protection should be also considered. The conventional resistive method can be used for soft-start. When the Boost circuit starts, the resistor with an appropriate rating is connected in series with the main power circuit. This resistor is shorted after the output capacitor is charged. In the implementation, the inductor current is sensed and compared with an over-current protection level. Once the sensed inductor current is higher than that level. A protection logic signal is generated and used to turn off the gate signal. At the same time, this protection logic signal is transferred to DSP so that the protection mode routine is activated. Over-voltage protection can be done in DSP software routine as both the output and input voltage are sensed. Once over-voltage condition is detected, the Boost converter is shut down.

The software flowchart to implement the proposed PFC control method is shown in Fig. 7. All the software is programmed by C code. The sampling frequency of the voltage loop is $6.4kHz$. It should be noted that $6.4kHz$ sampling frequency is high enough for the voltage loop, whose bandwidth is only $5\text{-}20Hz$ for regular PFC. Duty cycle calculation algorithm is performed in the interruption service routine (ISR). The interruption frequency is the same as the switching frequency, which is $160kHz$ in the implementation of this paper. With the assembly code for ISR, the switching frequency could be achieved as high as $300kHz$ based on a low cost, $40MHz$ clock frequency DSP.

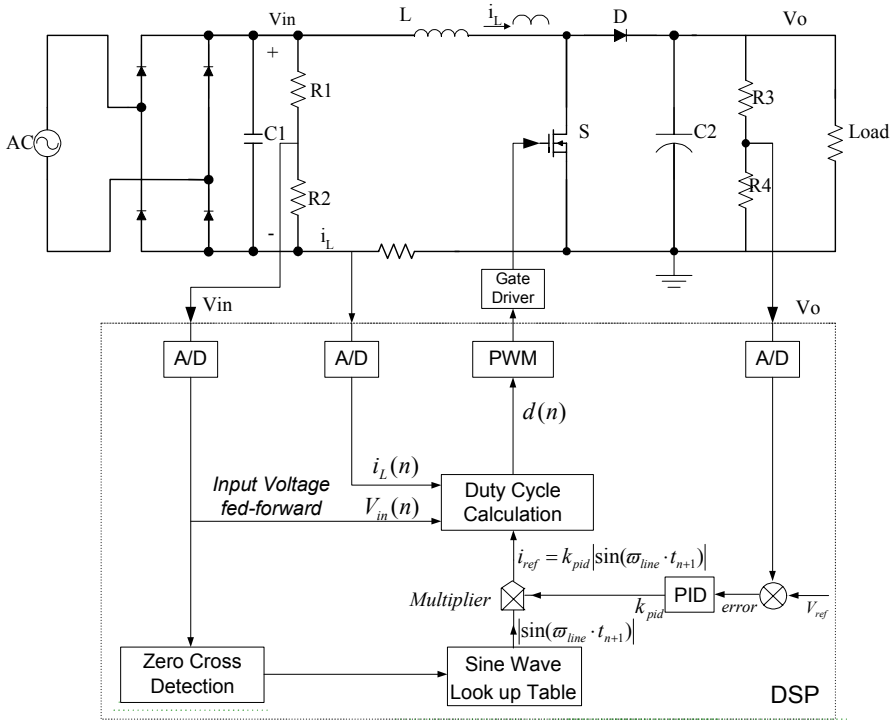


Fig. 5 DSP controlled PFC implementation

Fig. 6 Boost PFC circuit controlled by DSP evaluation board

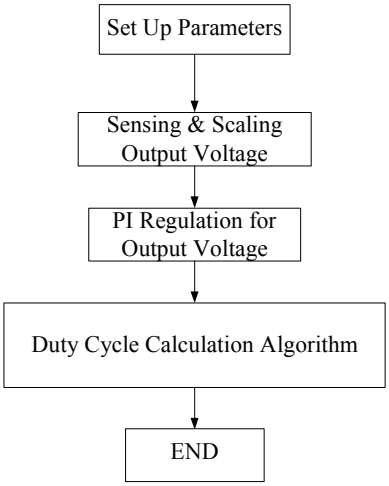


Fig. 7 Software implementation for proposed PFC control algorithm

V. EXPERIMENTAL RESULTS

The experimental results based on DSP implementation with a Boost topology have been done to verify the proposed PFC control method. The test operating parameters are the same as that used in section III. The performances in both the steady state and transient state are tested by the experimental results.

The input current and voltage waveforms for the full load (I_o=3A) under the steady state is shown in Fig. 8. The power factor in this situation is 0.996 and THD is 8.5%. The input current and voltage waveforms for two third load (I_o=2A) under the steady state is shown in Fig. 9. The power factor in this situation is 0.995 and THD is 9.7%. Test result shows that the proposed PFC control method can achieve near unity power factor in the steady state.

The input current waveforms under distorted input voltage condition are shown in Fig. 10. The input voltage is 110V and clipped at 85% peak value. The output voltage is 200V and load current *Io* is 3A. The power factor is 0.995 and THD is 9.85%. Test result shows that the proposed PFC control method can achieve sinusoidal input current waveform under non-sinusoidal input voltage condition.

The dynamic performance in transient state when the load current is changed from 2A to 3A and from 3A to 2A are shown in Fig. 11 and Fig. 12, respectively. The output voltage drop is 4.5V when the output power changed from 400W to 600W (load current I_o changed from 2A to 3A). The output voltage overshoot is 5V when the output power changed from 600W to 400W (load current I_o changed from 3A to 2A). The input current can maintain sinusoidal waveform in the load transient state. The setting time is about 150*mS* and the voltage loop bandwidth is about 15*Hz*.

The dynamic performance in transient state for step input voltage change is shown in Fig. 13 and Fig. 14, respectively. When the input voltage is changed from 110 to 95*V*, the output voltage drop in the transient state is about 2.7V. When the input voltage is increased from 95 to 110*V*, the output voltage overshoot in the transient state is 3V. The input current still maintains sinusoidal waveform in transient state. The voltage drop or overshoot to the step input change is small.

Some techniques have been explored to reduce the calculation requirement further and make the proposed PFC control method more practical. One of the techniques is that one duty cycle is calculated and serves for multiple (e.g., 2, 4,…) switching cycles. That means the frequency of interruption service routine (ISR) for calculation of the duty cycles is several times lower (e.g., ½, ¼,…) than the switching frequency. Therefore, the calculation requirement is reduced greatly. Table 1 shows the tests results on THD.

Table1 THD for single duty cycle serving in multiple switching cycles

Multiple switching cycles	1	2	4	8
Interruption frequency (*kHz*)	160	160/2	160/4	160/8
THD (Full Load I_o=3*A*)	8.5%	9.6%	8.8%	8.6%

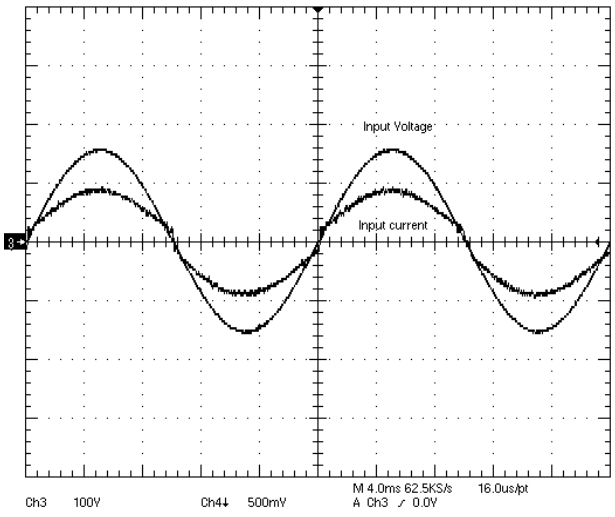


Fig. 8 Input voltage and current waveforms for full load

(*Io=3A, PF=0.996, THD=8.5%*)

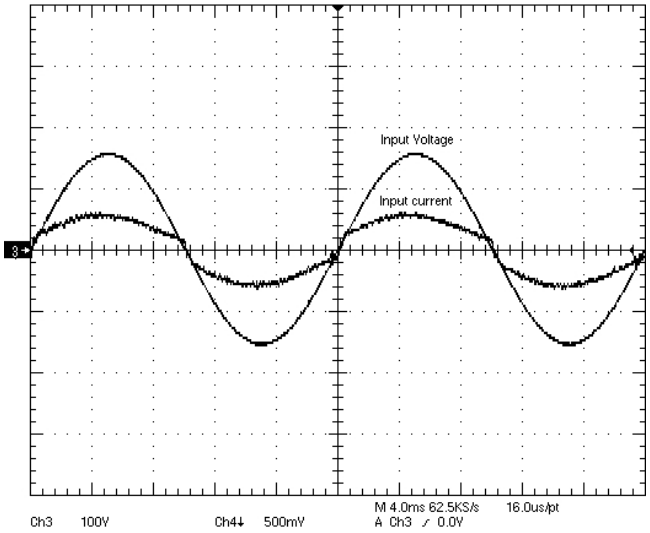


Fig. 9 Input voltage and current waveforms for two third load (*Io=2A, PF=0.995, THD=9.8%*)

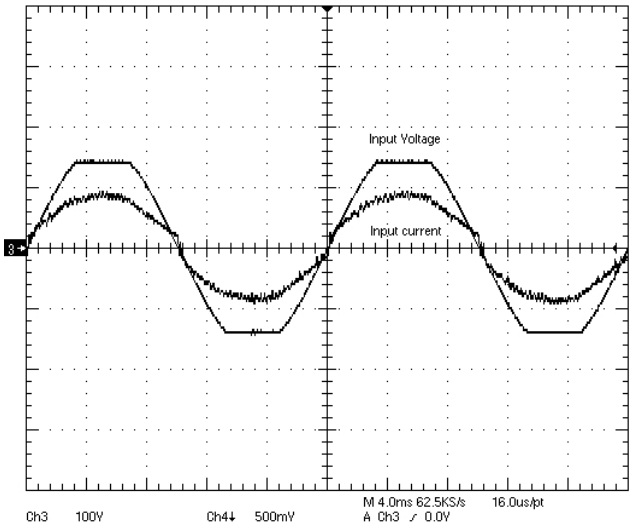


Fig. 10 Input current waveform for distorted input voltage

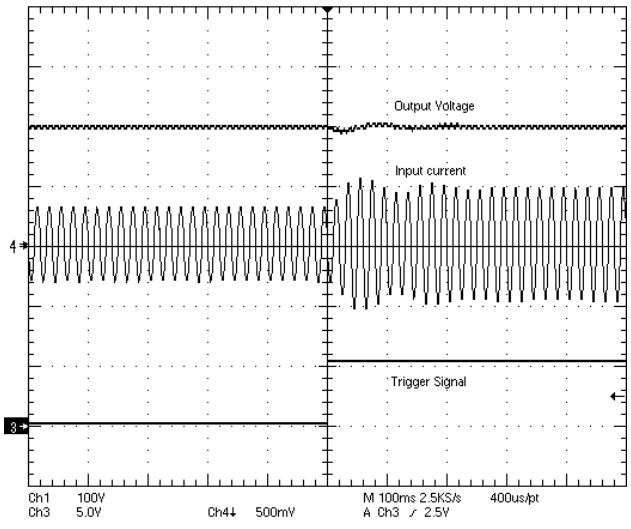


Fig. 11 Input current & output voltage waveforms in load transient state (Io changed from 2A to 3A,output voltage drop 4.5V)

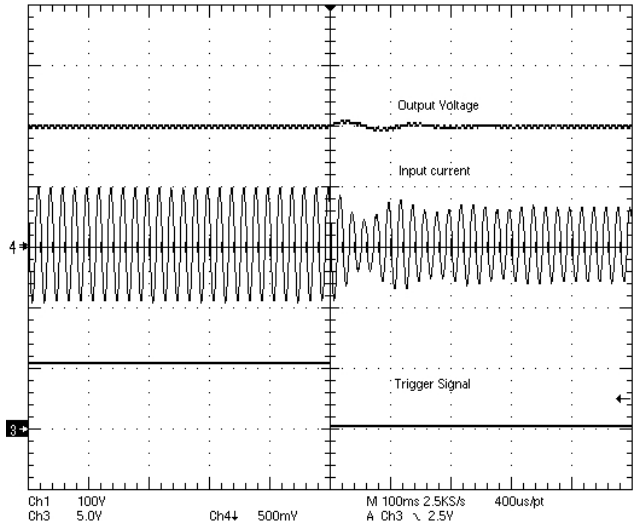


Fig. 12 Input current & output voltage waveforms in load transient state (Io changed from 3A to 2A, output voltage overshoot 5V)

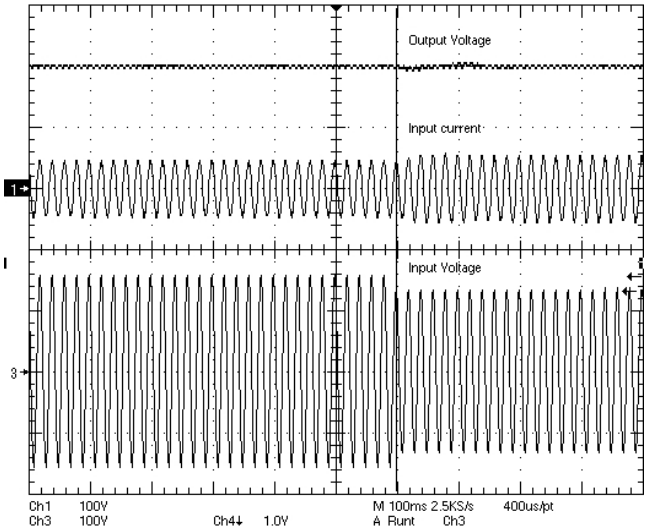


Fig. 13 Input current & output voltage for step input voltage change (V_{in} changed from110V to 95V, output voltage drop: 2.7V)

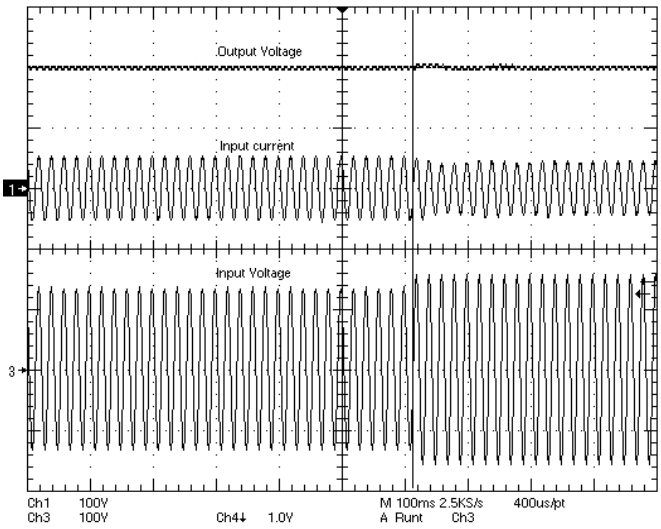


Fig. 14 Input current & output voltage for step input voltage change (V_{in} changed from 95 to 110V, output voltage overshoot: 3V)

VI. CONCLUSION

A new PFC control method based on direct duty cycle control is proposed. The duty cycle required to achieve unity power factor is calculated directly based on the reference current and sensed inductor current, input voltage and output voltage. For digital implementation, it requires only one multiplication and three addition operations so that the proposed PFC control method can be implemented by a low cost DSP, or a microprocessor to achieve high switching frequency. For analog implementation, a different control architecture is used to achieve unity power factor compared with other PFC control method. For both digital and analog implementation, the proposed PFC control method is simpler than commonly used average current mode control for PFC implementation. Yet same and better performance can be achieved.

Test results for a digital implementation show that the proposed method can achieve unity power factor under both steady and transient state. Sinusoidal input current can be achieved under non-sinusoidal input voltage condition. The proposed digital PFC control method can achieve good dynamic performance for load and input voltage change. The proposed conception can also be applied in other topologies, such as flyback, buck-boost, etc., to achieve unity power factor.

VII. REFERENCES

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