A Self Core Reset and Zero Voltage Switching Forward Converter Topology

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***Abstract*—A self core reset and zero voltage switching (ZVS) forward converter topology is presented in this paper. By employing a simple auxiliary circuit, the proposed topology is able to achieve self reset of the power transformer without the use of the conventional tertiary reset winding, and its main switch can be turned on and turned off under ZVS independent of line and load conditions. This simplifies the power transformer, and the switching losses are substantially removed to improve the overall efficiency. Steady state analysis of the circuit is performed. Based on the analysis, a design procedure is presented, and the effects of the circuit parameters on the flux excursion of the power transformer are investigated to make sure self reset can be achieved without increasing the core losses. Simulation and experiment on a 5 V, 100 W prototype circuit operated at 200 kHz are carried out to verify the design. About 5% higher overall efficiency is obtained in the prototype converter than in its conventional counterpart.**

***Index Terms*—Forward converter topology, power transformer, self-driven synchronous rectifiers, soft switching, zero voltage switching.**

I. Introduction

In THE conventional forward converter topology, the power transformer essentially requires a tertiary winding to reset the core. This makes the transformer structure more complicated than those of other single switch converter topologies, and it merely means higher cost in manufacturing the transformer. Furthermore, a transformer with more windings needs a bobbin requiring more pins, and a bobbin with more pins needs a larger core, therefore a larger core has to be used even though a smaller one satisfies the power requirement. This for sure increases the size of the transformer and eventually increases the overall size of the converter. Thus, the forward power transformer should be simplified.

Another shortcoming of the conventional forward topology is the hard switching operation. To reduce the size and increase the power density of the converter, the switching frequency is usually increased so that smaller sized mangnetics and capacitors can be employed. Unfortunately, to do so, the overall efficiency will be very low because of increased switching losses, and high power density can simply not be obtainable due to high cooling requirements. Besides, the di/dt in the hard switching converter is high, producing the EMI problems. Consequently, the conventional hard switching topology is not suitable for applications in advanced telecom and computer systems. To solve these problems, soft switching techniques are normally used.

Several modified forward topologies have been developed in recent years [1]–[17]. Among them, the resonant reset forward (RRF) and active reset/clamp forward (ARF) topologies operate with simplified power transformers that do not need the tertiary reset winding. In order to optimize its performance, the RRF generally works with variable switching frequency. Unfortunately, this is not applicable to applications like computer systems, because the switching ripples and harmonics are varying at variable switching frequencies and they are very hard to filter out. Then, the digital display of a computer, for instance, will appear flickering and swimming. The RRF can also operate at fixed switching frequency, but the penalty for this is the high voltage stress on the main switch. For a typical input voltage range of 35 V to 75 V, the voltage stress would be close to 200 V. In addition, although RRF usually achieves soft switching at full load, it loses soft switching at light load. The hard switching will locally cause thermal problems on the main switch. This leads to high cooling requirement on the switch.

The most serious problem with RRF is the difficulty to drive the synchronous rectifier (SR). If SR is driven directly from the transformer winding, the body diode of the synchronous MOSFET will conduct. This is because, due to resonance, the voltage waveform has a sinusoidal shape during the reset interval. This waveform has a slow slope at the beginning and end of the reset interval, and consequently reducing the gate drive voltage level below the threshold of the freewheeling synchronous FET. Thus, the body diode of the freewheeling synchronous FET has to conduct during these periods, reducing the efficiency of the synchronous rectifier stage. Furthermore, as the body diode latches in, its slow reverse recovery would cause spikes. Extra circuit can be added to overcome these problems. However, first of all, the circuit becomes more complicated. Secondly, the two SR's will cross conduct. It should be noted that SR must be properly driven over wide input voltage and entire load current condition, not just at a specified operating point. When the switching frequency is increased, the problem becomes even worse.

ARF overcomes many of RRF's drawbacks—it operates at a constant frequency and in zero voltage switching (ZVS). However, to achieve ZVS, normally a saturable inductor is added, and that brings nonlinear property and makes design complex. ZVS may also be achieved by lowering the magnetizing inductance of the power transformer, but this increases conduction

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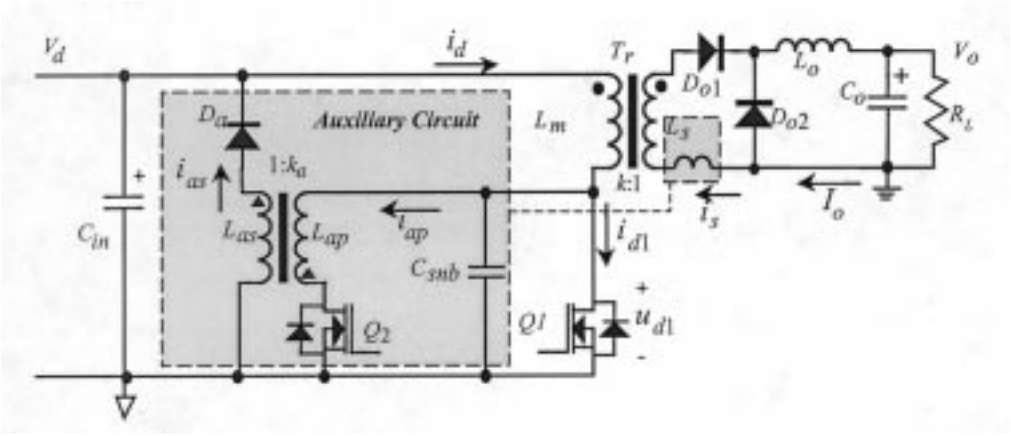


Fig. 1. Proposed forward converter topology. No tertiary reset winding.

losses. Circulating current in the clamp circuit results in additional conduction losses. Besides, ARF, as well as other modified forward topologies reported in recent years, also suffers from at least one of the following drawbacks.

1) Variable pulse width gating pattern with controllable dead time for the reset/clamp switch must be generated,
2) When the clamp switch uses an n-channel MOSFET, its gate drive must be isolated from the main switch. When a p-channel MOSFET is used as the clamp switch, theoretically there is no need of the gate drive isolation. However, an additional, negative bias voltage ($-Vcc$) for the gate drive circuit is required to turn off the p-type device.
3) ZVS is lost under light load conditions.
4) Current mode control is not applicable in topologies like ARF, making the compensation hard in closing the loop and causing slow dynamic response, and
5) Patent related legal issues create difficulties in their applications.

In order to overcome these drawbacks, this paper presents an improved ZVS forward converter topology with self core reset. In this topology, a simple auxiliary circuit is employed. The auxiliary circuit consists of a small switch as well as a few passive components. With this auxiliary circuit, the proposed topology is able to achieve self-reset of the power transformer without the use of the conventional tertiary reset winding, and its main switch can be turned on and turned off under ZVS independent of line and load conditions. This simplifies the power transformer, and the switching losses are substantially removed to improve the overall efficiency under all operating conditions. Besides, the gating of the auxiliary switch is in fixed pulse width, and there is no need of gate drive isolation. All these simplify the design of control and gate drive circuits. Moreover, the feedback loop design is flexible; it can be accomplished in either voltage mode or current mode control, though it will not be discussed in this paper.

In this paper, steady state analysis of the circuit is performed to understand its operation and hence to optimize its performance. A design procedure is given based on the analysis. The effects of the circuit parameters on the magnetic flux excursion of the power transformer are investigated to make sure self reset can be achieved without increasing the core losses. Simulation and experiment are carried out to verify the analysis and design using a 35–75 V to 5 V, 100 W, 200 kHz prototype converter. About 5% higher overall efficiency is obtained in the prototype converter than in its conventional counterpart.

II. Circuit Description

Fig. 1 shows the proposed ZVS forward converter topology. It can be divided into two functional sub-circuits. One is the auxiliary circuit that is inside the shaded block. The other one outside the block is the power circuit, which employs a simplified transformer without the tertiary reset winding.

The power circuit is comprised of the following components:

1) T_r, the two-winding power transformer with a magnetizing inductance L_m and a turns ratio of k;
2) Q_1, the main switch;
3) D_{o1} and D_{o2}, the output rectifiers that can be replaced with synch FETs;
4) L_o and C_o, the output filter;
5) R_L, the load.

The auxiliary circuit consists of the following components:

1) Q_2, an auxiliary switch;
2) C_{snb}, a snubber capacitor for the main switch;
3) L_s, a current limiting inductor, which is inserted into the secondary side of T_r;
4) L_{ap} and L_{as}, two coupled inductors;
5) D_a, a blocking diode.

The auxiliary circuit fulfills a threefold function, namely

1) it provides the ZVS conditions for the main switch Q_1 at both turn-on and turn-off, thereby eliminating the switching losses;
2) it resets the core of the power transformer at desired constant frequency;
3) it provides the zero current switching (ZCS) condition for the auxiliary switch Q_2 at turn-on.

III. Steady State Analysis

Following assumptions are made to perform the steady state analysis:

1) the input and output voltages are V_d and V_o, respectively;
2) the output power is P_o;
3) L_m is much greater than both L_{ap} and k^2L_s;

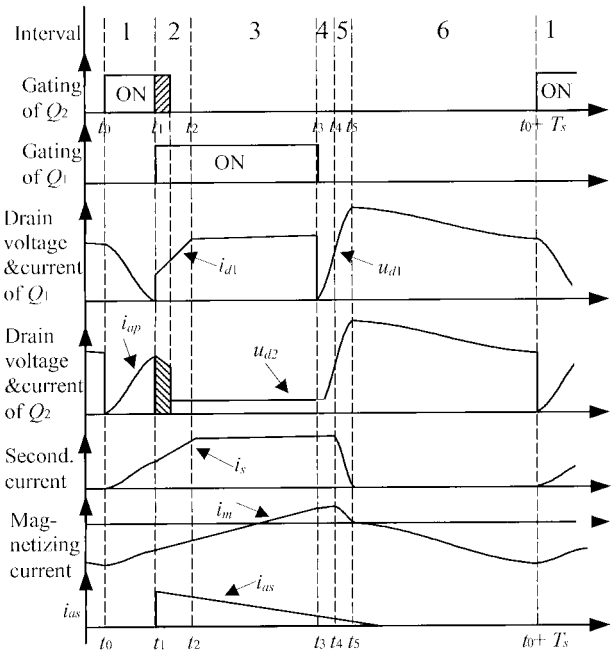


Fig. 2. Key waveforms. Each cycle can be divided into six intervals.

4) L_o and C_o can be considered as infinite;
5) the converter is operated in the continuous conduction mode (CCM).

Fig. 2 shows key waveforms of the steady state operation of the proposed converter topology. Each switching cycle can be divided into six intervals.

A. Interval 1 ($t_0 \le t < t_1$)

At the beginning of this interval, Q_2 is turned on under the zero current switching (ZCS) condition because of the series inductor L_a. As Q_2 is ON, a resonant network comprising C_{snb}, L_{ap}, L_m and L_s is formed. Fig. 3(a) shows the equivalent circuit.

The drain-to-source voltage of Q_1 is found given by

$$u_{d1}(t) = \frac{L_{ap}}{L_{ap}+k^2L_s} V_d + \left(\frac{k^2L_s}{L_{ap}+k^2L_s}+\alpha\right) \cdot V_d \cos[\omega_1(t-t_0)] \quad (1)$$

where α is a factor by which u_{d1} is higher than V_d at t_0, and

$$\omega_1 \approx \sqrt{\frac{1}{C_{snb}} \cdot \frac{L_{ap}+k^2L_s}{k^2L_{ap}L_s}}. \quad (2)$$

The current flowing through L_{ap} and Q_2 is found to be

$$i_{ap}(t) = \frac{V_d}{L_{ap}+k^2L_s}(t-t_0) + \left(\frac{k^2L_s}{L_{ap}+k^2L_s}+\alpha\right) \cdot \frac{V_d}{\omega_1 L_{ap}} \sin[\omega_1(t-t_0)]. \quad (3)$$

This current stores energy in form of a static magnetic field in the core of the coupled inductors. Owing to the assigned polarity of L_{as} and L_{ap}, D_a is reverse biased and it blocks any current through L_{as}.

When u_{d1} falls below the value of V_d, L_m starts to see a positive voltage. Thus, the magnetizing current and the secondary current start to rise and they are determined, respectively, by

$$i_m(t) = I_{m0} + \frac{k^2L_sV_d}{L_m(L_{ap}+k^2L_s)}(t-t_0) - \left(\frac{k^2L_s}{L_{ap}+k^2L_s}+\alpha\right)\frac{V_d}{\omega_1 L_m}\sin[\omega_1(t-t_0)] \quad (4)$$

$$i_s(t) = \frac{kV_d}{(L_{ap}+k^2L_s)}(t-t_0) - \left(\frac{k^2L_s}{L_{ap}+k^2L_s}+\alpha\right) \cdot \frac{V_d}{k\omega_1 L_s}\sin[\omega_1(t-t_0)] \quad (5)$$

where I_{m0} is the value of the magnetizing current of T_r at t_0.

At the end of this interval, C_{snb} is totally discharged and u_{d1} becomes zero. As the inductor current through L_{ap} must continue, the body diode of Q_1 latches in to give the current a path. Thus, u_{d1} is clamped at zero, and this provides ZVS condition for Q_1 to turn on.

The magnetizing current, the secondary current and the auxiliary circuit current that are governed by (4), (5), and (3), respectively, reach the values defined by

$$I_{m1} = i_m(t_1) \quad (6)$$

$$I_{s1} = i_s(t_1) \quad (7)$$

$$I_{ap} = i_{ap}(t_1). \quad (8)$$

B. Interval 2 ($t_1 \le t < t_2$)

At the beginning of this interval, Q_1 is turned on under zero voltage condition and Q_2 can be turned off now or shortly after. The equivalent circuit is shown in Fig. 3(b).

When Q_2 is turned off, i_{ap} is stopped abruptly and the voltage polarity across L_{as} is changed. This forces D_a to conduct, feeding the energy that was stored in L_{ap} during Interval 1 back the input dc line. This current is determined by

$$i_{as}(t) = \sqrt{\frac{L_{ap}}{L_{as}}}\, I_{ap} - \frac{V_d}{L_{as}}(t-t_1). \quad (9)$$

As D_a conducts, L_{as} sees the input voltage. Due to coupling of the coupled inductors, Q_2 will see a voltage stress as given by

$$V_a = \sqrt{L_{ap}/L_{as}}V_d. \quad (10)$$

On the other hand, as Q_1 is ON, L_m sees a constant voltage V_d, and i_m rises linearly as governed by

$$i_m(t) = \frac{V_d}{L_m}(t-t_1) + I_{m1}. \quad (11)$$

The secondary current keeps rising as governed by

$$i_s(t) = \frac{V_d}{kL_s}(t-t_1) + I_{s1}. \quad (12)$$

At the end of this interval, i_s reaches the output inductor current I_o. It is seen that this interval reduces the effective duty ratio of the main switch.

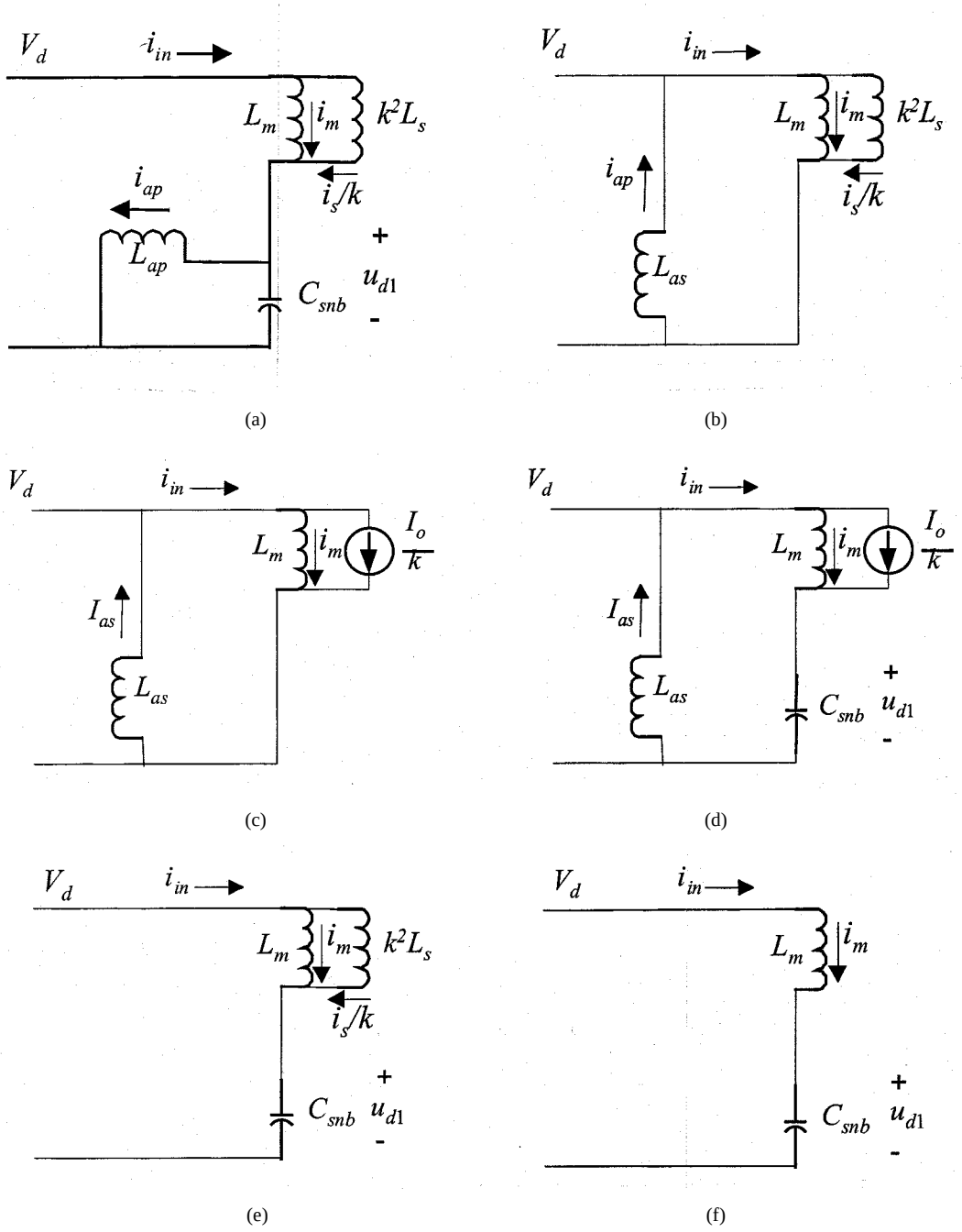


Fig. 3. Equivalent circuits during each interval. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6.

C. Interval 3 ($t_2 \leq t < t_3$)

At the beginning of this interval, the secondary current reaches the value of the output inductor current, i.e.,

$$i_s(t) = I_o \tag{13}$$

where I_o is the load current, namely P_o/V_o. Then, D_{o2} is reverse biased and D_{o1} starts to carry the total output inductor current, and the power circuit transfers power to the load as in the conventional forward converter. The equivalent circuit is shown in Fig. 3(c).

The magnetizing current is still governed by (11) as L_m still sees the constant voltage V_d. At the end of this interval, the on period of the main switch is completed so as to regulate the output voltage. At this time ($t = t_3$), the magnetizing current governed by (11) reaches a value defined by

$$I_{m2} = i_m(t_3). \tag{14}$$

D. Interval 4 ($t_3 \leq t < t_4$)

At the beginning of this interval, Q_1 is turned off. The drain current starts to drop fast to zero while the voltage across Q_1 starts to rise at a relatively slow rate determined by C_{snb}. By selecting a proper value of C_{snb}, the overlap between the drain current and drain voltage is greatly reduced and a ZVS turn-off is essentially achieved for Q_1.

Before u_{d1} reaches V_d, the secondary winding still sees a positive voltage equal to $V_d - u_{d1}$. Thus, D_{o1} is still forward biased to conduct the total output inductor current as in (13). The equivalent circuit is shown in Fig. 3(d).

The drain-to-source voltage of Q_1 is now determined by

$$u_{d1}(t) = V_d - V_d \cos[\omega_2(t-t_3)] + \frac{kI_{m2} + I_o}{k\omega_2 C_{snb}} \sin[\omega_2(t-t_3)] \tag{15}$$

where

$$\omega_2 = 1/\sqrt{L_m C_{snb}} \tag{16}$$

and the magnetizing current is now determined by

$$i_m(t) = \frac{V_d}{\omega_2 L_m} \sin[\omega_2(t-t_3)] + \left(I_{m2} + \frac{I_o}{k}\right) \cdot \cos[\omega_2(t-t_3)] - \frac{I_o}{k}. \tag{17}$$

This interval ends when u_{d1} reaches V_d. Thus, the duration of this interval is given by

$$t_4 - t_3 = \frac{1}{\omega_2} \arctan\left(\frac{k\omega_2 C_{snb} V_d}{kI_{m2} + I_o}\right). \tag{18}$$

At the end of this interval, the magnetizing current governed by (17) reaches a value defined by

$$I_{m3} = i_m(t_4). \tag{19}$$

E. Interval 5 ($t_4 \le t < t_5$)

At the beginning of this interval, u_{d1} rises above V_d and L_m starts to see a negative voltage equal to $V_d - u_{d1}$. Due to this negative voltage, the secondary current through L_s decreases. Since the current through L_o is almost constant, D_{o2} is forced to conduct to compensate for the decreasing current through D_{o1} and L_s. The equivalent circuit for this interval is shown in Fig. 3(e).

The drain-to-source voltage of Q_1 is now governed by

$$u_{d1}(t) = V_d + \frac{kI_{m3} + I_o}{k\omega_3 C_{snb}} \sin[\omega_3(t-t_4)] \tag{20}$$

where

$$\omega_3 = 1 \Big/ \sqrt{\frac{k^2 L_s L_m}{k^2 L_s + L_m} C_{snb}} \approx 1 \Big/ \sqrt{k^2 L_s C_{snb}} \tag{21}$$

It is found that this voltage will reach the peak value determined by

$$V_{peak} = V_d + \frac{kI_{m3} + I_o}{k\omega_3 C_{snb}}. \tag{22}$$

The magnetizing and secondary currents are now governed, respectively, by

$$i_m(t) = \frac{kL_s(kI_{m3} + I_o)}{L_m} \cos[\omega_3(t-t_4)] + \frac{k(L_m - k^2 L_s) I_{m3} - k^2 L_s I_o}{kL_m} \tag{23}$$

$$i_s(t) = (kI_{m3} + I_o) \cos[\omega_3(t-t_4)] - kI_{m3}. \tag{24}$$

This interval completes at $t = t_5$ when i_s drops to zero. From (24) the duration of this interval is found to be

$$t_5 - t_4 = \frac{1}{\omega_3} \arccos\left(\frac{kI_{m3}}{kI_{m3} + I_o}\right). \tag{25}$$

At the end of this interval, the magnetizing current governed by (23) reaches a value as given by

$$I_{m4} = i_m(t_5) \tag{26}$$

and the drain voltage of the main switch governed by (20) reaches a value given by

$$V_1 = u_{d1}(t_5). \tag{27}$$

F. Interval 6 ($t_5 \le t < t_0 + T_s$)

At the beginning of this interval, the residual current through L_s reaches zero. As blocked by D_{o1}, the current through L_s cannot reverse to continue the resonance. Thus, L_m and C_{snb} form a new resonance circuit. The equivalent circuit for this process is shown in Fig. 3(f).

It is found that

$$u_{d1}(t) = V_d + (V_1 - V_d) \cos[\omega_2(t-t_5)] + \frac{I_{m4}}{\omega_2 C_{snb}} \sin[\omega_2(t-t_5)] \tag{28}$$

$$i_m(t) = \frac{V_d - V_1}{\omega_2 L_m} \sin[\omega_2(t-t_5)] + I_{m4} \cos[\omega_2(t-t_5)]. \tag{29}$$

At the end of this interval, one switching cycle is completed. The drain voltage returns to the same value as at the beginning of this cycle, and this defines the factor α by

$$\alpha = \frac{u_{d1}(T_s) - V_d}{V_d}. \tag{30}$$

The magnetizing current also returns to the same value as at the beginning of this cycle, namely (29) should yield

$$i_m(T_s) = I_{m0}. \tag{31}$$

Thus, the core of the power transformer T_r is reset. A new cycle now begins.

In summary, at the beginning of each cycle, the auxiliary circuit discharges the snubber capacitor in Interval 1, it feeds the discharged energy back the input dc line afterwards, and in this way it helps remove and save the turn-on switching losses of the main switch. Power is delivered to the output in Interval 3 in the same way as in a conventional forward converter. The snubber capacitor slows down the rise of the drain voltage of the main switch in Interval 4 and 5 to substantially remove its turn-off losses. Finally, through the rest of the cycle, the power transformer is reset through the resonance undertaken by L_s, L_m and C_{snb}.

A fixed gating pattern for the auxiliary switch is chosen on purpose to simplify the design and implementation, otherwise the proposed topology would suffer from the same drawbacks as does the active reset forward (ARF) in the complex control and gate drive circuit design. With this fixed gating pattern, ZVS can not be achieved arbitrarily. Careful attention must be paid

to selecting and matching the auxiliary circuit components in order to guarantee ZVS under the entire operating range, which will be discussed below.

IV. Design Procedure and the Effects of the Circuit Parameters on the Flux Excursion

Based on above analysis, a design procedure to select components of the auxiliary circuit of Fig. 1 is given in this section. The selection criteria for the power circuit are not shown herein as it is a conventional circuit for which the design has been extensively published in the literature.

Assume that the following principal parameters are known.

1) $D_{\max}$: maximum duty cycle of Q_1;
2) f_s: switching frequency;
3) L_m: magnetizing inductance of T_r;
4) k: the turns ratio of T_r;
5) V_o: output voltage;
6) I_o: full load current;
7) $V_{d\min}$ and $V_{d\max}$: the minimum and maximum input voltage, respectively.

A. Design Procedure

1) Selection of the Auxiliary Duty Ratio: Basically, the successful reset of the power transformer by any means requires the volt-second balance between the magnetizing and demagnetizing process. When the reset interval is shorter, the power switch as well as the rectifier D_{o1} will suffer from higher voltage stress. To avoid excess voltage stress, the design must leave adequate time for resetting. As the auxiliary duty ratio steals some time from the permitted resetting duration, a large D_{aux} will narrow the reset duration. To guarantee the least reset time not to be less than the maximum magnetizing time, the fixed duty ratio of the auxiliary switch shall be limited by

$$D_{aux} < (1 - 2D_{\max}). \tag{32}$$

The auxiliary duty ratio may also be limited by the PWM chip like UC3855, where it is less than 0.1.

2) Coupled Inductors L_{ap} and L_{as}: As seen from (1), to guarantee ZVS, u_{d1} must always drop to zero at the end of Interval 1. This can only be achieved if the following condition is satisfied:

$$k^2 L_s \geq \frac{1-\alpha}{1+\alpha} L_{ap}. \tag{33}$$

Obviously, it is difficult to satisfy (33) over all the operating conditions, because α that is determined by (30) is not a fixed parameter but depending on the line and load conditions. For simplicity in design, let

$$L_{ap} = k^2 L_s. \tag{34}$$

L_{as} should be large enough to suppress the turn-off voltage stress on Q_2 as described in (10). But L_{as} should also be limited such that the release of the stored energy after Interval 1 can finish within one switching cycle. This limits L_{as} by

$$L_{as} \leq \left(\frac{1-D_{aux}}{D_{aux}}\right)^2 L_{ap}. \tag{35}$$

3) Current Limiting Inductor L_s: As seen from (5), a large L_s will sufficiently slow down the rise of the secondary current in Interval 1 and that permits C_{snb} to discharge completely. For successful depletion of charges on C_{snb}, the actual current direction through the capacitor must be flowing out. This requires the derivative of (1) to be negative, which leads to

$$\omega_1 \frac{D_{aux}}{f_s} \leq \pi. \tag{36}$$

Substituting (2) and (34) into (36), it yields the following limitation on the selection of L_s:

$$L_s > \frac{2D_{aux}^2}{k^2 \pi^2 f_s^2 C_{snb}}. \tag{37}$$

However, L_s reduces the effective duty ratio of the main switch as shown in Interval 2. Excessive duty ratio reduction will require a larger output inductor to meet the output ripple specification. To limit the duty ratio reduction, as seen from (12), L_s must be limited by

$$L_s < \frac{V_d}{kI_o f_s}\,\delta \tag{38}$$

where δ is the permitted reduction of the effective duty ratio. A practical design should limit δ below 10%.

4) Selection of the Snubber Capacitor C_{snb}: The value of C_{snb} determines the rise time of the drain voltage of Q_1 at its turn-off, as described in (15). For a very short duration, as the magnetizing current is negligible when compared to the load current, it is approximated that

$$\Delta u_{d1}(t) \approx \frac{I_o}{kC_{snb}}(t - t_3). \tag{39}$$

It indicates that C_{snb} should be so chosen to limit u_{d1} below V_d within an expected rise time t_r that usually is about a few hundred nanoseconds. Then, by (39), the capacitor should satisfy the following equation:

$$C_{snb} > \frac{I_o}{kV_{d\min}} t_r. \tag{40}$$

On the other hand, as seen from (1) and (2), C_{snb} must also satisfy the following equation to guarantee u_{d1} to drop to zero by the end of Interval 1

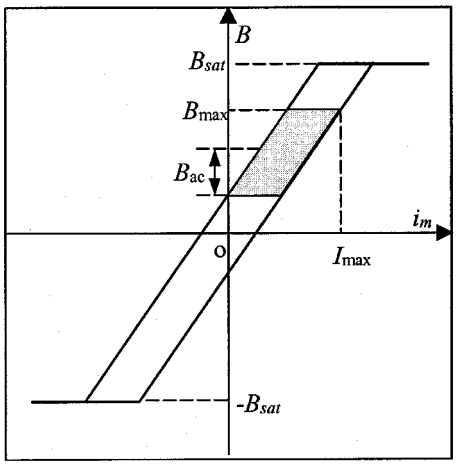
$$C_{snb} \leq \frac{4(L_{ap} + k^2 L_s)}{\pi^2 k^2 L_s L_{ap}}. \tag{41}$$

5) Auxiliary Switch Q_2: In selection of Q_2, trade off should be made between the least inherent capacitance and the least on-resistance in order to result in the least total losses in Q_2. Its current rating should be able to handle the discharging current given by (3), and its voltage rating is determined by (22).

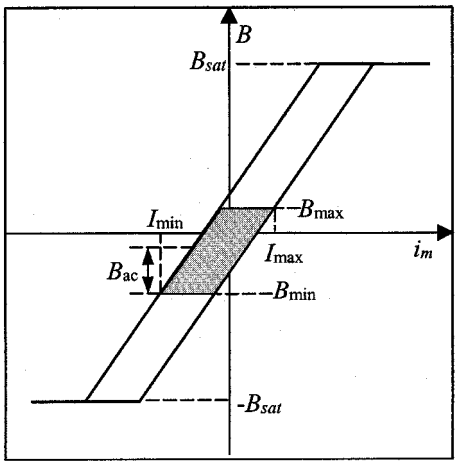
6) Blocking Diode D_a: It is a fast recovery diode with low forward voltage drop. The maximum reverse voltage it sustains is given by

$$V_{R\_Da} = V_d + \sqrt{\frac{L_{as}}{L_{ap}}}\, V_{peak}. \tag{42}$$

It should be able to handle a current given by (9).



(a)



(b)

Fig. 4. Comparison of the flux excursion and the hysteresis loop traversed in the conventional forward transformer and the self reset transformer. (a) Conventional transformer. (b) Self reset transformer.

B. Flux Swing and the Effects of Circuit Parameters

Fundamentally, the flux density is related to the magnetizing current by

$$B(t) = \frac{L_m}{NA_e}\, i_m(t) \tag{43}$$

where

B flux density;
N number of turns of the magnetizing winding;
A_e effective cross section area of the core.

In magnetic design, the flux excursion should be kept well below the saturation point. Then, the flux excursion and the magnetizing current swing are linearly proportional. Fig. 4(a) shows the flux excursion in the conventional forward type transformer, and as long as the circuit is in CCM, this excursion remains almost the same under different line and load conditions. In contrast, for the self reset transformer, as seen in (17), (23) and (29), the line and load conditions indeed affect the swing of magnetizing current. This causes the shift of the flux excursion, as shown in Fig. 4(b), leaving it biased in either up or down direction by a dc flux that is determined by the operating conditions. Therefore, during operation, the flux excursion in the self reset transformer may shift over the first and third quadrants of the hysteresis loop. The most important thing is to keep the shift from the saturation point that does not exceed 3000 Gauss for most ferrite core materials.

Another important issue is the core and copper losses. The core losses are determined by the area of the hysteresis loop that the flux excursion traverses, and they are approximately proportional to the square of the ac peak flux density. As seen in (4), (11), (17), (23), and (29), increasing L_m will narrow the swing range of magnetizing current, and it reduces the ac peak flux density and the core losses as well. This can be done by adding more turns in the magnetizing winding. However, it increases the copper losses as well as the transformer size and weight. Hence, a compromise in selecting L_m should be made to minimize the total losses in magnetics, and it is well treated in conventional design. A question here is whether the conventional design suits for the self reset transformer.

Fortunately, the core losses as well as the copper losses in the self reset transformer does not differ much from that in the conventional forward transformer, if they are designed the same except for the absence of the tertiary reset winding in the former. The reason is as follows. The ac peak flux is almost half of the swinging up (or equally the swing down) excursion of the flux. When the main switch is ON, the flux swings up linearly, and this swinging up excursion is proportional to the input dc voltage and the duty ratio of the main switch. If the operating conditions are the same, the ac peak flux in both the self reset transformer and a conventional one will be the same, although the dc bias flux may differ. Hence, the core losses will be the same in both transformers. The copper losses are determined by the power that the transformer transfers. Both conventional transformer and the self reset one will suffer from almost the same copper losses for the same output power. Some negligible difference in copper losses may exist due to their different bias in magnetizing current, which is comparatively much less than the load current. In short, the self reset transformer can achieve self reset without sacrificing copper and core losses. Therefore, the self reset transformer can follow the well developed conventional design procedure.

Above all, the flux excursion should be kept from saturation. To guarantee this, it must be investigated how the flux excursion varies with operating conditions as well as the circuit parameters. Should the core self reset, (31) must be satisfied. Based on (4), (11), (17), (23), (29), (31), and (43), the effects of each parameter on the magnitude and range of the swinging flux can be determined accordingly.

Fig. 5 shows the flux excursion as functions of V_d, I_o, L_m, L_s, and C_{snb} in the prototype circuit that is shown below. These curves are generated with MathCAD based on the analysis presented in this paper. The flux swings back and forth over the range bounded by $B_{\max}$ and $B_{\min}$, and the excursion varies with the circuit parameters and operating conditions.

It is seen from these curves that the excursion moves toward the first quadrant from the third quadrant of the B–H loop when the load decreases. The reason is as follows. As shown in (22), V_{peak} is proportional to the load current, and it overcomes the

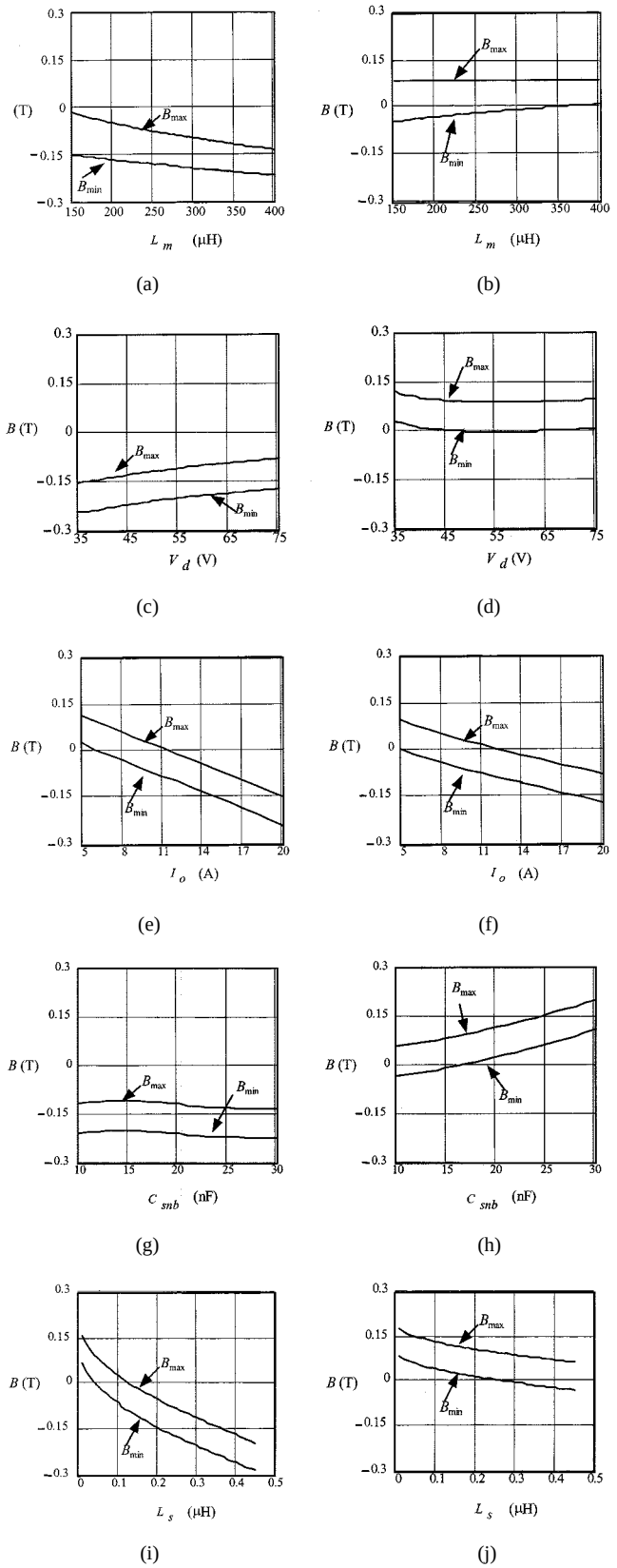


Fig. 5. Flux excursion as function of different parameters in the prototype circuit. The flux density swings back and forth between the two boundaries, $B\max$ and $B\min$. The output voltage $Vo = 5$ V, switching frequency is 200 kHz. (a) B versus L_m at full load. (b) B versus L_m at light load. (c) B versus V_d at full load. (d) B versus V_d at light load. (e) B versus I_o at high V_d. (f) B versus I_o at low V_d. (g) B versus C_{snb} at full load. (h) B versus C_{snb} at light load. (i) B versus L_s at full load. (j) B versus L_s at light load.

TABLE I
PRINCIPAL PARAMETERS OF THE EXAMPLE CIRCUIT

parameter		parameter	
$V_{d\,\min}$, $V_{in\_\max}$	35V, 75V dc	D_{o1}/D_{o2}	MTP75N05*
P_o	100W (V_o=5V,I_o=20A)	Q_3	IRF510
$D_{\min}/D_{\max}$	0.2 / 0.42	Controller	UC3855AN
f_s	200kHz	D_{aux}	0.1
L_m	320μH	L_s	0.3μH
k	3:1	L_{ap}/L_{as}	3μH/96μH
L_o/C_o	12 μH / 400μF	C_{snb}	16nF
C_{in}	100μF	Q_2	IRF634
Q_1	IRF640*	D_a	HFA08TB

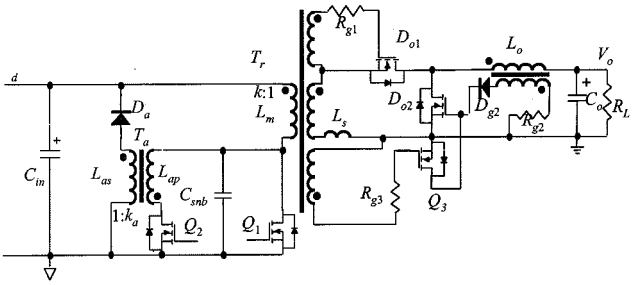


Fig. 6. The prototype converter. It employs self-driven synchronous rectifiers reported in [18].

input voltage V_d to drive the magnetizing current i_m to drop back during the reset process. At light load, V_{peak} is lower, resulting in a weaker driving force to reverse i_m.

It is also seen in these curves that at full load, the excursion traverses only the third quadrant of the B–H loop. It means a negative magnetizing current. Benefited from this negative current are the slightly reduced copper losses, since the current stress on the primary side is likely reduced.

In detail, Fig. 5(a) and (b) show that the flux excursion as a function of the magnetizing inductance L_m. These curves also point out that a larger L_m reduces the excursion range and hence the core losses. However, at full load, the excursion drifts farther away from the origin as L_m increases. It implies that a very large L_m will not only increase the conduction losses and size of the transformer due to more turns in the winding but also drive the transformer into saturation.

Fig. 5(c) and (d) show the flux excursion as a function of the input voltage V_d. It is seen that, as V_d increases, though the excursion remains almost independent of V_d at light load, it shifts toward the first quadrant of the B–H loop under full load condition. The reason can also be found in (22); at higher V_d, V_{peak} produces a relatively weaker force to drive the magnetizing current to drop back during the reset process.

Fig. 5(e) and (f) show the flux excursion as a function of the output current I_o. It is seen that, as the load decreases, the excursion shifts toward the first quadrant. This does not increase the conduction losses at light load, because of the reduced load current.

Fig. 5(g) and (h) show the excursion as a function of the snubber capacitor C_{snb}. It is seen that, at full load, the excursion is almost independent of the snubber value. But at light load, the larger the snubber, the higher the excursion moves up into the first quadrant of the B–H loop. The reason can still be

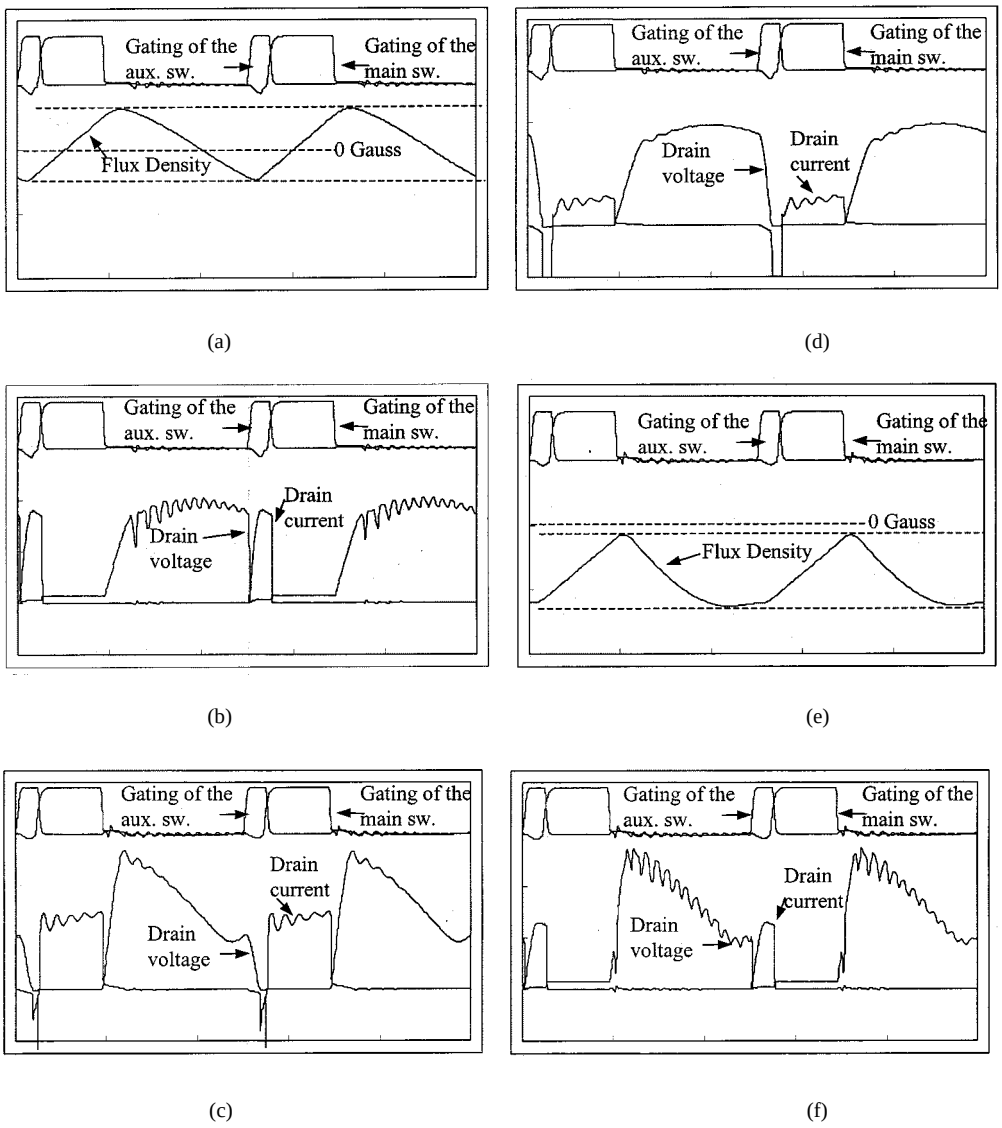


Fig. 7. Typical key waveforms of simulation results. (a) Flux excursion at light load. (b) Q_1 waveforms at light load. (c) Q_2 waveforms at light load. (d) Flux excursion at full load. (e) Q_1 waveforms at full load. (f) Q_2 waveforms at full load.

found in (22); the peak voltage of the main switch is in inverse proportion to C_{snb}. A larger C_{snb} results in a lower V_{peak} and a weaker force to drive i_m back during the reset process. Thus, the value of C_{snb} should be limited again in this sense, although a larger C_{snb} is preferable in removing the turn-off losses of the main switch.

Fig. 5(i) and (j) show the excursion as a function of the current limiting inductance L_s. It is seen that a larger L_s will move the excursion deeper into the third quadrant of the B–H loop. It is because, as seen in (21) and (22), a larger L_s results in a smaller ω_3 and hence a higher V_{peak}, producing a stronger force to drive i_m to drop back during the reset process. The curves also show that, when L_s is too small, the excursion move fast up into the first quadrant of the B–H loop, and saturation may happen. This just demonstrates the necessity of the role that L_s plays in the self reset topology. Hence, to avoid saturation, L_s should be limited on both ends so that excursion does not reach the saturation point either in the first quadrant or the third quadrant.

C. A Design Example

A prototype of 35 V to 75 V dc to 5 V dc 100 W converter operating at 200 kHz has been built. Synchronous rectifiers are used in the output stage. Design of the auxiliary circuit follows the procedure given above, and the selection of components is refined by consulting the flux swing curves in Fig. 5. The components and principal parameters of the circuit are listed in Table I.

Fig. 6 shows the schematic of the prototype circuit with self-driven synchronous rectifiers [18] in the output stage. The main switch uses two paralleled IRF640 to half the conduction losses, and the auxiliary switch uses a lower power rating IRF634. Two paralleled low R_{dsON} MOSFET's (MTP75N05, 9 mΩ) are used for each of the synchronous rectifiers to further improve the conversion efficiency. The gate drive for synchronous rectifier D_{o1} is generated by a winding coupled to T_r, and for D_{o2} by a winding coupled to L_o. A small MOSFET switch Q_3 (IRF510)

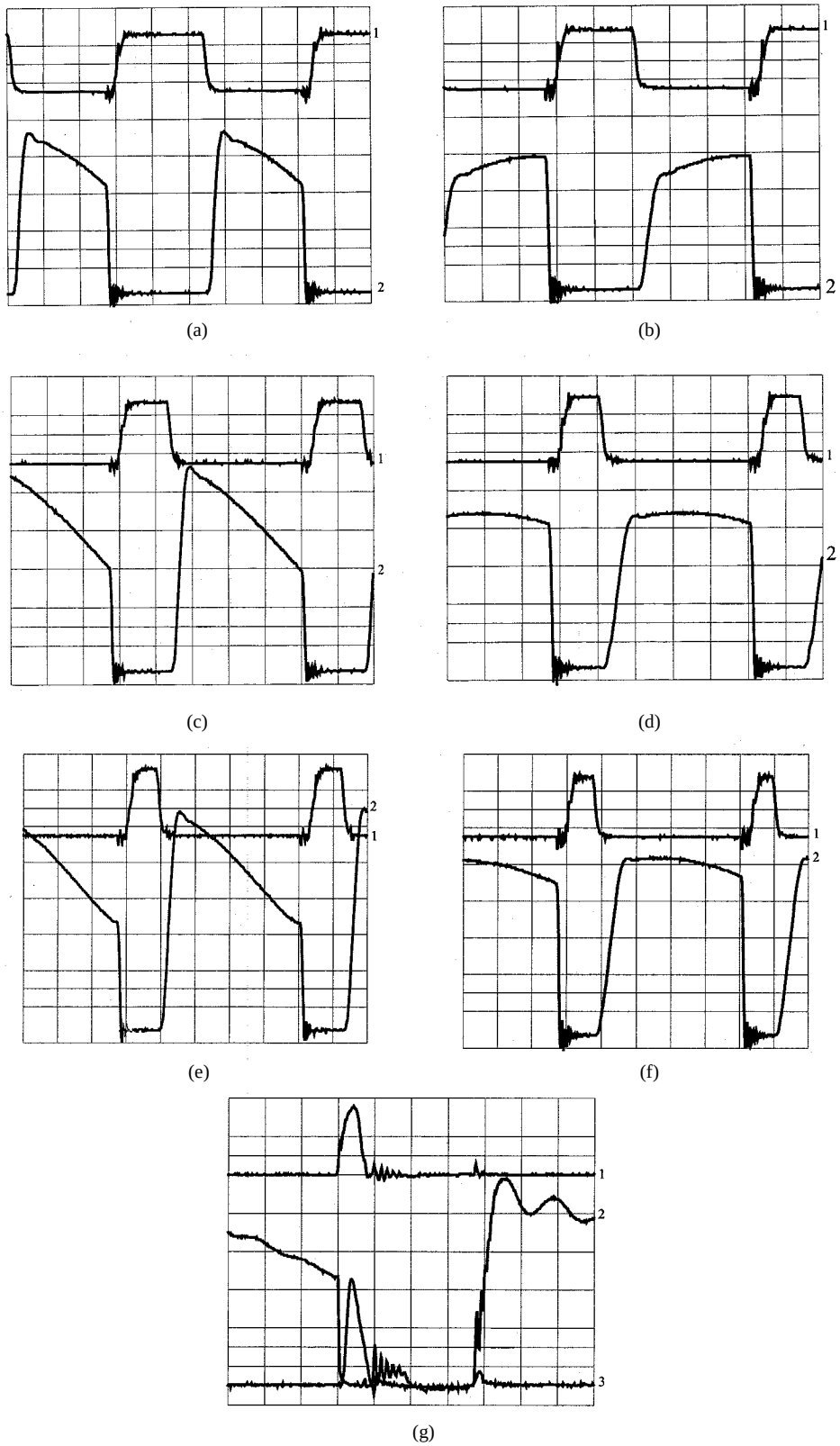


Fig. 8. Experimental results: key waveforms at different operating conditions. Trace 1: gating. Trace 2: drain voltage. Trace 3:drain current. $fs = 200$ kHz. Scales: gating—10 V/div., drain voltage—20 V/div., drain current—1A/div., timing (except in 7 g)—1 μs/div. (a) $Q_i, V_d = 35$ V, $P_o = 100$ W. (b) $Q_i, V_d = 35$ V, $P_o = 25$ W. (c) $Q_i, V_d = 35$ V, $P_o = 100$ W. (d) $Q_i, V_d = 55$ V, $P_o = 100$ W. (e) $Q_i, V_d = 75$ V, $P_o = 100$ W. (f) $Q_i, V_d = 75$ V, $P_o = 25$ W. (g) $Q_i, V_d = 55$ V, $P_o = 100$ W, 0.5 MS/div.

helps to fast turn off D_{o2}. The Schottky diode D_{g2} (1N5819) blocks the excessive negative gate voltage during the off time of D_{o2}.

In this prototype circuit, an ETD29 core is selected for the power transformer. The core material is PC40 with an effective permeability of 1500, and the maximum flux excursion is

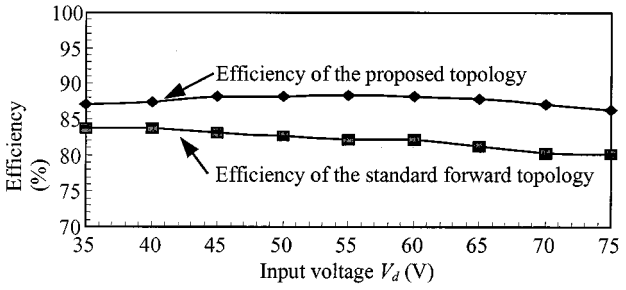


Fig. 9. Overall efficiency versus input voltage. $Po = 100$ W, $Vo = 5$ V, $fs = 200$ kHz. Synchronous rectifiers are employed in both ZVS converter and the standard forward converter.

chosen at 880 Gauss. Litz wires are used for the two power windings. The primary winding with 12 turns yields a magnetizing inductance of about 320 μH. At the switching frequency of 200 kHz, the core losses are about 0.6 W at 100°C, and the copper losses are about 0.9 W at full load. As shown in Fig. 5, when $C_{snb} = 16$ nF, $L_s = 0.3$ μH, the flux excursion is well bounded within the saturation points of 3000 Gauss.

The coupled inductors L_{ap} and L_{as} are made of an air gapped SP41408 pot core, and L_s takes the advantage of the secondary winding leakage. The total losses by the coupled inductors are less than 0.5 W.

V. Experimental and Simulation Results

Using the prototype circuit, simulation and experiment are carried out. Some characteristic results are shown below.

Fig. 7 shows typical key simulation waveforms obtained using Pspice. It shows, at either full load or light load, that i) the magnetizing current returns to the same value after each cycle, that means the core is successfully reset, ii) the main switch has ZVS at both turn-on and off, and iii) the auxiliary switch has a ZCS turn-on.

Fig. 8 shows key waveforms of the experimental results under different operating conditions. The drain current of the main switch is not shown for the reason that inserting a current probe into the power circuit requires a long wire hook and it interferes with the normal operation of the circuit. But it is safe to judge that ZVS is always achieved in the main switch under all those operating conditions, because the gate signal always arrives after the drain voltage drops to zero and finishes before the drain voltage rises from zero. Though unable to measure the flux swing, the successful self reset of the core can be proven by the steady state operation under all those operating conditions.

Fig. 9 shows the overall efficiency as a function of input voltage. It is seen that the efficiency is the highest when the input voltage is 55 V that is the middle point of the input voltage range, and it reduces slightly at both ends of the input voltage range. The reasons are as follows.

At a lower input voltage, higher rms current flows for a given output load, thus the conduction losses are higher. At a higher input voltage, although the conduction losses in the power circuit decrease, the auxiliary circuit will be slightly less efficient to feed the removed switching losses back into the input dc line. It is because the snubber stores more energy to discharge at a higher input voltage, and higher auxiliary current is required as shown in (3). This increases the conduction losses in the auxiliary circuit. Besides, as the auxiliary switch has a hard switching turn-off, more switching losses will be resulted from a higher input voltage. All these reduce the overall converter efficiency at higher input voltage, although these losses are very small as compared to the load current. At middle point of the input voltage range, either the conduction losses in the power circuit or the losses in the auxiliary circuit do not go excessive, thus the converter has the highest overall efficiency.

Above all, the proposed self reset ZVS topology has about 5% higher efficiency at full load than does the conventional hard switching forward converter.

VI. Conclusions

The proposed forward converter topology employs a simplified power transformer that can self reset without the use of the conventional tertiary reset winding. This reduces the cost and size of the transformer without increasing the core losses and thus not sacrificing the overall circuit efficiency. Simulation and experimental results show successful core reset and guaranteed ZVS under various operating conditions. Better than 5% increase in efficiency is obtained with the proposed topology as compared to the conventional forward converter.

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