A New Current Sensing Scheme for Zero-Voltage Switching Phase-Shifted Bridge Converter

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Abstract:
The current sense schemes for Zero-Voltage Switching, Phase-Shift Bridge converter are discussed. A new current sense scheme is proposed that can reliably and accurately sense the output inductor current and at the same time prevent the power transformer and current sense transformer from saturating in both steady state and transient conditions. The operation of the circuit is discussed. Computer simulation and experimental results are presented to confirm the analysis.

1. Introduction

The bus voltage for a typical telecom power system is 48V DC. For median to high output power application, a two-stage power converter is usually used to obtain this 48V DC bus from AC utility line. One stage is an AC-to-DC converter that converts the AC utility voltage (110V or 220V) into a high voltage DC (usually 400V dc). Power factor correction is achieved by this AC-to-DC converter. The other stage is a DC-to-DC converter that converts this high DC voltage into 48V DC bus. Electrical isolation between AC line and 48V DC bus is realized in this DC-to-DC converter.

The output of the Boost converter contains fairly large low frequency ripple. For 60Hz line frequency, the ripple frequency is 120Hz. The peak-to-peak ripple voltage could be as high as 10% of the DC value. This low frequency ripple has to be attenuated significantly by the DC-to-DC converter so that the 48V DC bus can meet the low frequency noise requirement for telecom application. This is sometimes called DBrnc requirement.

DBrnc requirement is used to describe the noise that human ear can hear. The frequency it covers is from a couple of hundred Hertz up to 3KHz. If the 120Hz ripple is not filtered out, the 48V will have this 120Hz noise and the human will hear this noise in their telephone set because the 48V is used to power the telephone set directly.

For medium to high power output application, Zero-Voltage Switching Phase-Shift Bridge converter is used for DC-to-DC conversion because of its advantages [1-4]. Current mode control is usually needed to achieve high enough attenuation for low frequency input noise and fast transient response.

In section 2 of this paper, various existing current sense schemes are discussed. Their advantages and disadvantages are also analyzed. In order to overcome these problems, a new current sense scheme is proposed in section 3. The operation of the new scheme is analyzed. Computer simulation results (in section 4) and experimental results (in section 5) are presented to confirm the analysis and the feasibility of the scheme. Section 6 is conclusion.

2. Existing Current Sensing Schemes

Fig. 1 shows the topology of the Zero-Voltage-Switching (ZVS) Phase-Shifted Bridge converter and various locations to sense the output inductor current. The leakage inductance L_{lk} is used to help achieve ZVS for the primary MOSFETs. In current mode control, the output filter inductor current (I_L) should be sensed. For the Phase-Shifted Bridge converter, there are several locations where the current sense transformer (CT) can be inserted as discussed below. In Fig.1, the secondary side of the current sense transformers is not shown for simplicity.

2.1 Secondary Side Current Sensing:

The first choice is to put a current sense transformer at secondary side of the power transformer in series the rectifier diode, shown in Fig.1 as CT11 and CT12, where CT11 and CT12 are the primary windings of the current sense transformer. When diode D1 is conducting, the inductor current is sensed through the winding CT11 and when diode D2 is conducting, the inductor current is sensed through winding CT12. When both diodes are conducting, the current information is not needed. When the current goes through D1 reaches the control command, Icon, MOSFETs S1 is turned off and S3 is turned on after a short dead time. When the current through D2 reaches Icon, S3 is turned off and S1 is turned on after a short dead time.

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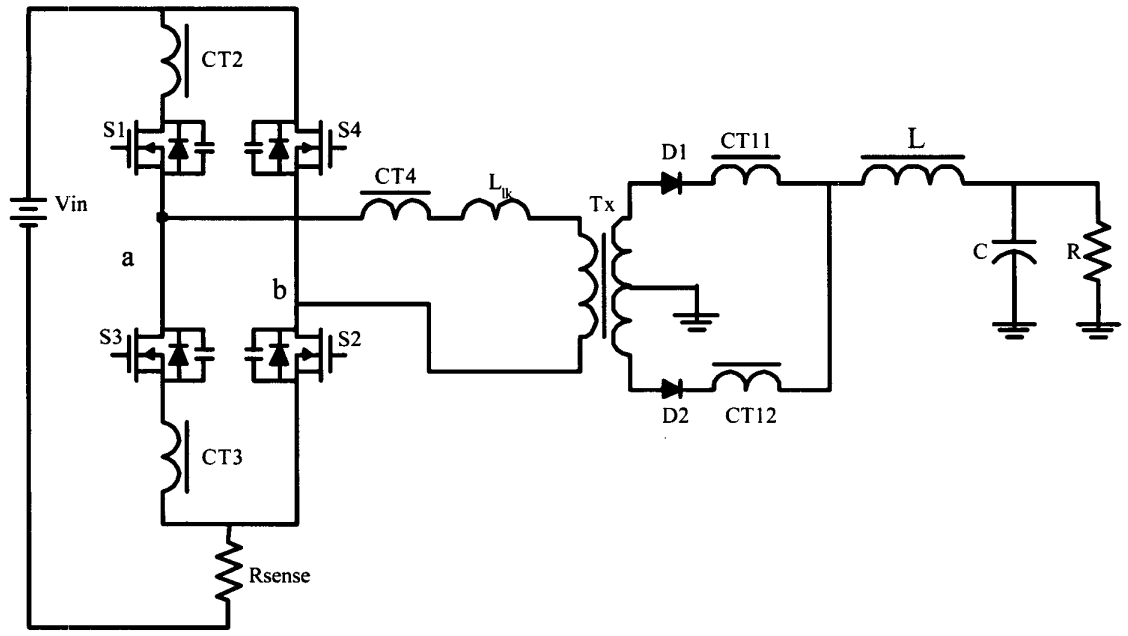

Fig.1 Locations to Sense the Output Inductor Current in Phase-Shift Bridge Converter

In this way, the inductor current can be sensed accurately. The problems of this scheme are: (a) it can not protect the primary MOSFET from over current, (b) it can not avoid DC current through the magnetizing inductor of the power transformer, (c) it is usually difficult to assemble the current sense transformer because of high current through the primary winding of current sense transformer.

2.2 Using Current Sense Resistor

Another choice is to use current sense resistor in series with primary MOSFET, as shown in Fig.1 by resistor Rsense. The major problems of this scheme are (a) another stage of amplifier is usually needed to increase the voltage level across Rsense because the value of Rsense is usually very small to reduce the power loss and (b) large common mode noise appears at the input of the current sense circuit. This is because in the practical design, in order to reduce EMI noise coupling, a common mode filter is usually needed between the output of the AC-to-DC stage and the input of the Phase-Shift Bridge converter. The ground is usually selected at the negative point of the AC-to-DC output.

2.3 Using Two Current Sense Transformers

Another scheme is to use two current sense transformers. One connected in series with S1, shown as CT2 in Fig.1 and the other is connected in series with the S3, shown as CT3 in Fig.1. The outputs of these two transformers are added together to get the complete inductor current information. When the current through S1 reaches control signal, Icon, S1 is turned off to end the energy transfer interval for the first half cycle. When the current through S3 reaches control signal, Icon, S3 is turned off to end the energy transfer interval for the second half cycle.

In addition to the fact that 2 current sense transformers are needed, the major problem of this scheme is that complicated circuit is needed to reset the core of the current sense transformers (CT2 and CT3). This is because there is a negative current flowing through the MOSFETs to discharge the output capacitor of S1 and S3 before they are turned on to achieve zero voltage switching. This negative current is also flowing through the current sense transformer. Because the amplitude and duration of this negative current is different for different load and line conditions, the current sense transformer cannot be reset automatically. Additional reset circuit has to be added. In addition, this scheme cannot provide over current protection for S2 and S4.

2.4 Current Transformer in Series with Power Transformer

The current sense transformer can also be connected in series with the power transformer, as shown in Fig.1 as CT4. All the problems in the above mentioned schemes could be avoided. Unfortunately, the major disadvantage of this scheme is that the current sense transformer or power transformer might be saturated. This is because the output voltage of the bridge, Vab = Va – Vb, will have some residual DC

value due to the difference of switching speed of each MOSFET, turn-on delay, dead time, as well as different output capacitor value of the MOSFETs. This DC value will cause saturation of either the current sense transformer or power transformer.

Therefore, a good current sense scheme is needed to achieve reliable current mode control for the Zero-Voltage-Switching Phase-Shift Bridge converter.

3. Proposed Current Sensingcheme

From the above discussion, it is shown that if we can avoid the saturation of the current sense transformer or power transformer, connecting the current sense transformer in series with the power transformer is the best way to sense the inductor current. The circuit shown in Fig. 2 is thus proposed.

A DC blocking capacitor (C_B) is added in series with the power transformer (Tx). The current sense transformer (CT) is connected in series with the power transformer. The residual DC voltage is blocked by the capacitor and there will be no DC voltage across the power transformer, or the current sense transformer. Therefore, these transformers will not be saturated.

One concern with this arrangement is that the voltage across the DC blocking capacitor (C_B) could build up (or sometimes called walk away) under transient condition or unbalanced condition. If this condition happens, the DC voltage across C_B would become very large and the circuit could not operate properly.

It is shown from the following analysis that this situation will not happen. Fig.3 shows the steady state voltage waveform across the power transformer primary side (top trace) and steady state current through the primary winding of the power transformer (bottom trace), where Icon denotes the current control signal. The primary MOSFETs that are conducting are also indicated. When the primary current reaches the control signal, Icon, MOSFET S1 is turned off to end the energy-transferring interval and the circuit operates at freewheeling stage when S2 and S3 are on. The second half cycle is similar to the first half cycle.

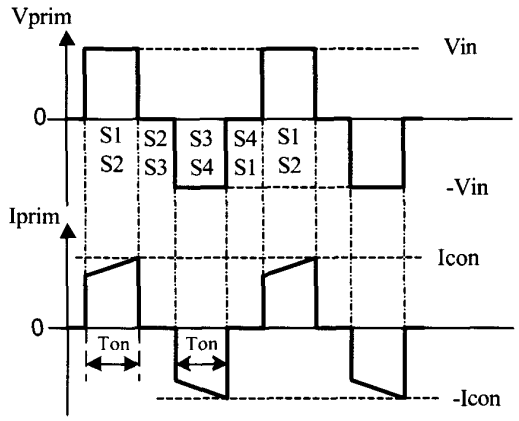

Fig. 3 Steady State Waveform of Vprim and Iprim

Assume for some unknown reason, the voltage across C_B (V_{CB}) deviate from its steady state value with the direction shown in Fig.4a (positive node at left and negative node at right). The operation under this unbalanced condition can be understood fairly well by the following four sub-periods in one switching cycle.

Following assumptions are made in the analysis,

(1) The dead time between the top and bottom switches are neglected and switching transition is not considered

(2) The impact of leakage inductance L_{lk} and current sense transformer are neglected.

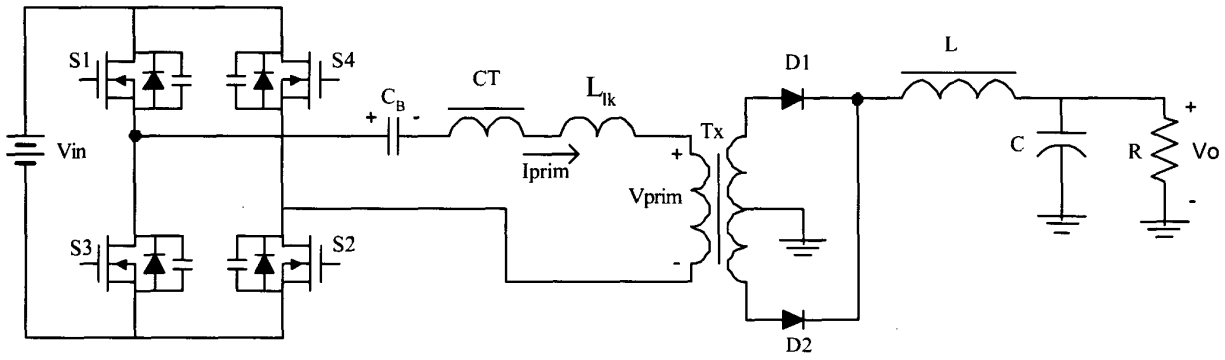

Fig.2 Proposed Scheme to Sense the Output Inductor Current

(3) The value of capacitor C_B is very large and its ripple voltage is neglected.

(4) The value of the output inductor is large and its current is continuous.

(5) In Fig.4, the thick lines represent the major current flow path.

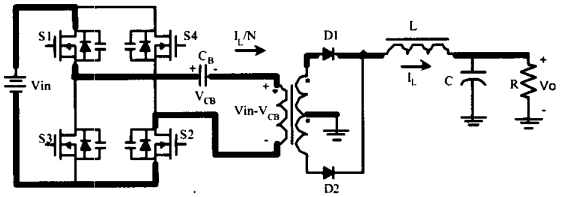

Fig.4a: S1 and S2 on

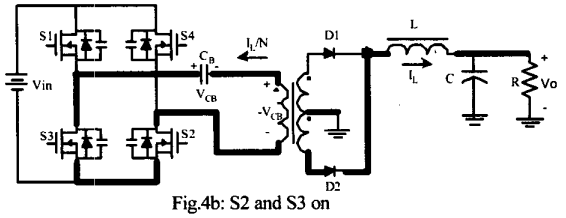

Fig.4b: S2 and S3 on

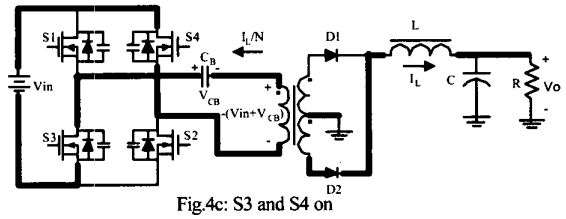

Fig.4c: S3 and S4 on

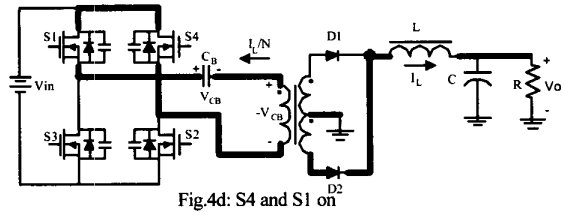

Fig.4d: S4 and S1 on

Fig.4 Equivalent Circuit Under Unbalanced Condition

Fig.5 gives the waveforms of the primary side voltage, Vprim, and primary side current, Iprim, at the unbalanced capacitor voltage condition. The devices that are on at each interval are also indicated.

Period 1: MOSFETs S1 and S2 conduct and diode D1 is also on. The equivalent circuit is shown in Fig.4a. The voltage across the primary side of the power transformer will be

$$V_{prim+} = V_{in} - V_{CB} \qquad (1)$$

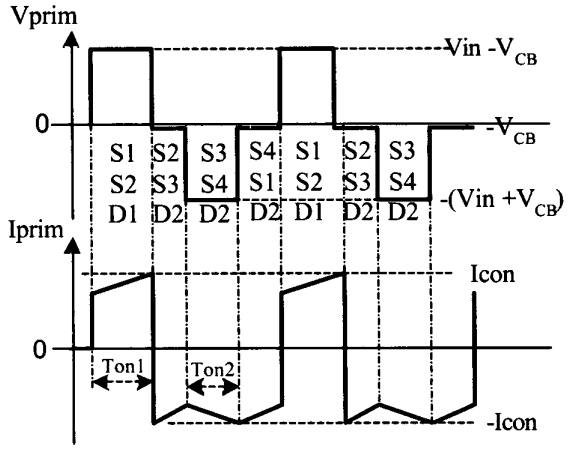

Fig.5 Waveforms of Vprim (top) and Iprim (bottom) at Un-Balanced VCB Condition

Because the voltage across the transformer primary side is lower, the rising slope for the output inductor is also smaller and it takes longer time for the reflected output inductor current to reach the current command, Icon. The energy transferring time for this half cycle, Ton1, is longer than that of the normal condition, Ton, when there is no V_{CB}. It is noted that Ton1 is smaller than half the switching period (Ton1 < 0.5*Ts).

Period 2: After S1 is turned off, S3 is on and the equivalent circuit is shown in Fig.4b. During this period, the capacitor voltage, V_{CB}, is applied to the primary side of the power transformer with the direction shown in Fig.4b (positive node at bottom and negative node at top). When this voltage is reflected to secondary side, the diode D2 will be forward biased and diode D1 is reverse biased. The output inductor current will flow through D2 only at this interval. The primary current is the reflected output inductor current and flows from right to left as shown in Fig.4b. During this interval, the energy is transferred from the capacitor C_B to the output.

Period 3: In the next half cycle, MOSFETs S3 and S4 are on and diode D2 is on as shown in Fig.4c. The transformer primary voltage is:

$$V_{prim-} = -(V_{in} + V_{CB}) \qquad (2)$$

Because the voltage across the transformer primary side is higher, the rising slope for the output inductor is larger and it takes less time for the reflected output inductor current to reach the current command, Icon. When the reflected output inductor current reaches -Icon, S3 is turned off. The energy transferring time for this half cycle, Ton2, is shorter than that of the normal condition, Ton.

Period 4: In this interval, S1 and S4 are on. The capacitor voltage V_{CB} is applied to the transformer primary side as indicated in Fig.4d. Again, diode D2 is forward biased and D1 is reverse biased and the output inductor current is reflected to the primary side and the primary side current flows from right to left as indicated in Fig.4d. The energy is transferred from C_B to the output during this interval.

From the above analysis, it is noted that under transient condition when V_{CB} deviate from its steady state value, diode D2 will conduct the output inductor current during free wheeling interval. Diode D1 is off during this time. This is different from the normal operation of the Phase-Shift Bridge converter where both D1 and D2 conduct during the free wheeling interval.

Because D2 conducts the full output inductor current for more than half the switching period and the negative current flows for more than half the switching period, the average value of the primary current is negative. This means that if the capacitor voltage deviates from its steady state value, it will be discharged by the reflected output inductor current and the voltage, V_{CB}, will reduce to its steady state value quickly.

Similarly, if the capacitor voltage deviates from its steady-state value into other direction (positive node at right and negative note at left), the diode D1 at the secondary side will be forward biased during the free wheeling interval when S1, S4 are conducting or S2, S3 are conducting. The capacitor voltage will be discharged by the reflected load current and its voltage will return to its steady state value quickly.

When the impact of the dead time and the leakage inductance are considered, the above conclusion will not change.

The above analysis shows that at the unbalanced condition when the voltage across the DC blocking capacitor, C_B, deviates from its steady state value, the circuit will force the capacitor to discharge and pull back the capacitor voltage to its steady state condition. The capacitor voltage will not walk away.

Therefore, in the proposed circuit shown in Fig.2, the residual DC voltage of Vab will be blocked by the capacitor C_B and neither the power transformer nor the current sense transformer will be saturated.

4. Computer Simulation Results

Computer simulation by SIMPLIS was done on a Zero-Voltage-Switching Phase-Shift Bridge converter with the DC blocking capacitor. Current mode control is used in the circuit. The input voltage is 400V. The output voltage is 54V. The output current is 20A. The power transformer has turns ratio of 6. The value of the DC blocking capacitor is C_B = 5uF. The output inductor value is 10uH. The switching frequency is 125KHz.

Fig. 6 shows the steady state waveforms for the DC blocking capacitor voltage, V_{CB}, (top trace) and the magnetizing inductor current, Imag (bottom trace). It shows that at steady state, the DC voltage across capacitor is about -45mV (with peak-to-peak value of 2V). In actual circuit, the average value will be a little bit bigger because of more severe unbalanced conditions.

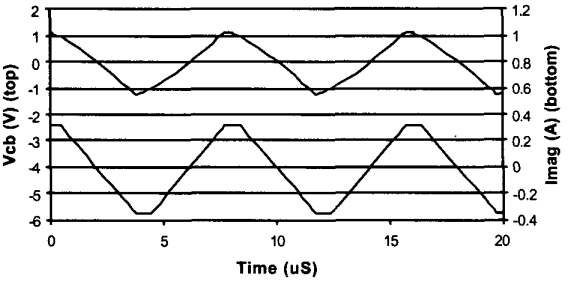

Fig.6 Steady State Waveforms for V_{CB} (top) and Imag (bottom)

The steady state waveforms for the primary voltage (Vprim, top trace) and primary current (Iprim, bottom trace) of the transformer are shown in Fig.7. Because of slightly unbalanced condition, during free wheeling interval, the diode current is not balanced and this unbalanced condition is reflected in the unbalanced waveform of the primary current during free wheeling interval.

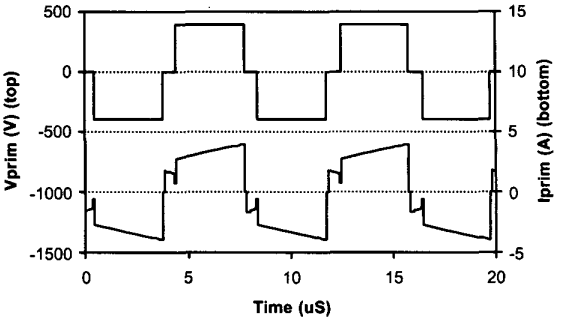

Fig. 7 Steady State Waveform for Vprim (top trace) and Iprim (bottom trace)

Computer simulation is also done for transient condition. When the capacitor voltage is forced to deviate from its steady state value of 1Vpk to 12Vpk at Time = 110uS, it settles down to 1Vpk again fairly quickly. Fig.8 shows the waveform of the capacitor voltage V_{CB} (upper trace) and the response of the magnetizing current (lower trace). The wave-

forms shows that under transient condition, the capacitor voltage and the magnetizing current will settle down to its steady state condition quickly. The capacitor voltage will not walk away.

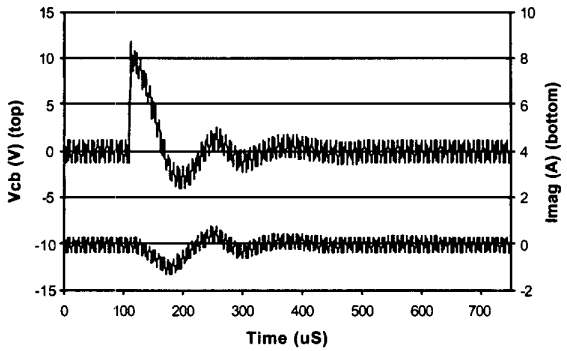

Fig.8 Response of V_{CB} (top) and Imag (bottom) at Transient Condition

Fig.9 gives the detailed waveform for the primary voltage (top trace) and primary current (bottom trace) immediately after the capacitor voltage step. It is noticed that before the capacitor voltage step, the waveform is same as those shown in Fig. 7. Immediately after V_{CB} transient (which happens at T = 110uS), the primary voltage is a small negative value during the free wheeling intervals when S1 and S4 are conducting or S2 and S3 are conducting. The primary current is the reflected inductor current (negative value) during these intervals. It is clear that the average value (over one switching cycle) of the primary current is negative because the negative portion of the current lasts longer than the positive one. This is same as the conclusion from the analysis in the previous section.

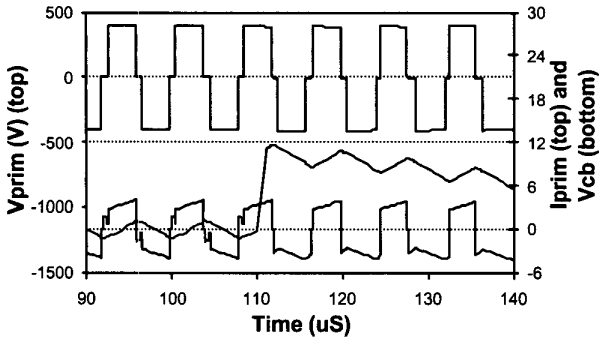

Fig.9 Detailed Waveforms of Vprim (top), V_{CB} (bottom step line) and Iprim (bottom) After the Transient

The above simulation results show that the capacitor voltage will not walk away under transient condition. Actually, it will settle down to its steady state value quickly. The capacitor is discharged by the reflected load current.

5. Experimental Results

Hardware prototype is also built to confirm the feasibility of the proposed techniques and to confirm the analysis results.

A Phase-Shift Bridge Converter under current mode control was built. A DC blocking capacitor is added in series with the power transformer and the current sense transformer is also connected in series with the power transformer. The prototype circuit is same as that shown in Fig. 2. The input voltage is 400V and the output voltage is 54V. The maximum output current is 50A.

The steady state voltage across the DC blocking capacitor at light load (10A) is shown in Fig.10 (channel 1). It is noted that the average value of V_{CB} is about –0.7V and the peak-to-peak value is about 5V.

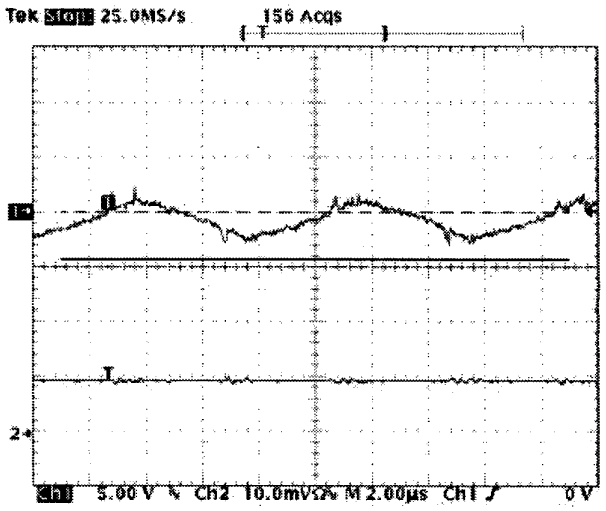

Fig.10 DC Blocking Capacitor Voltage Waveform at Light Load: 10A (Channel 1)

At heavy load (50A), the waveform of the DC blocking capacitor is shown in Fig.11 (channel 1). At this time, the peak-to-peak voltage is increased to about 13V and the average value becomes –3.5V.

The above waveforms show that there is a DC voltage component across the DC blocking capacitor due to unbalanced bridge voltage. The higher the load current, the more unbalance it becomes and the higher the average value of V_{CB} (amplitude wise) because the impact of all the parasitic components becomes larger at heavy load.

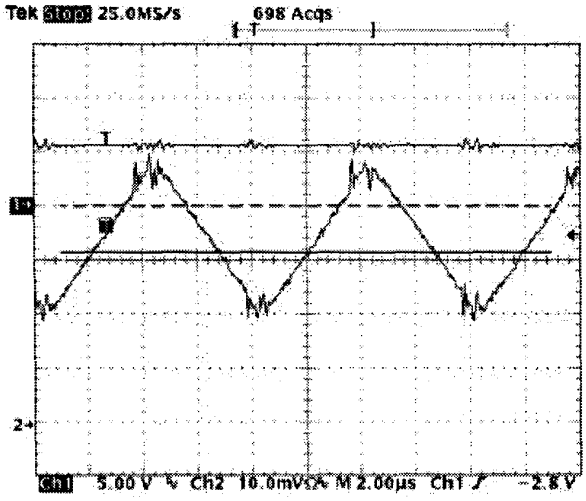

Fig.11 DC Blocking Capacitor Voltage Waveform at Heavy Load: 50A (Channel 1)

Because it is difficult to change the capacitor voltage suddenly in the experimental setup, the load current step change is used as the mean to introduce the large transient. Fig. 12 shows the measured waveform for the DC blocking capacitor voltage (channel 1) and the load current (channel 2) when the load current has a sudden change from 50A to 2A. The waveform shows that at large transient condition, there is no over shoot or undershoot for the capacitor voltage. The capacitor voltage will not walk away.

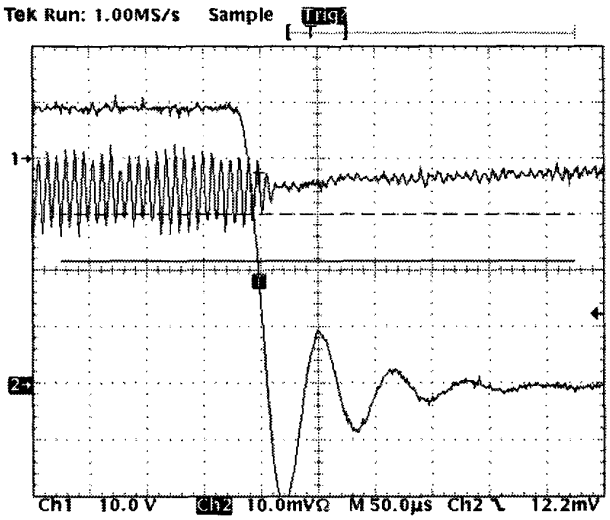

Fig.12 Measured Capacitor Voltage (Channel 1) Under Large Load Current Transient (Channel 2)

5. Conclusion

The existing techniques to sense the output inductor current for Zero-Voltage-Switching Phase-Shift Bridge converter are discussed. Their advantages and disadvantages are analyzed.

A new current sense scheme is proposed for Zero-Voltage Switching Phase-Shift Bridge converter. A DC blocking capacitor is connected in series with the primary side of the power transformer to prevent either power transformer or current sense transformer from the saturation. Both the computer simulation and experimental results show that the capacitor voltage will not walk away and neither the power transformer, nor the current sense transformer will saturate. Using this scheme, the output inductor current can be sensed accurately and all the MOSFETs can be protected from over current. Current mode control can be implemented reliably and accurately. The 120Hz ripple can be attenuated significantly to meet the DBrnc requirement.

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