Posting Date: October 05, 2021
Closing Date: November 12, 2021

The Department of Electrical and Computer Engineering in the Faculty of Engineering and Applied Science at Queen’s University requests applications from suitably qualified candidates interested in teaching the following undergraduate course in the 2021-22 session.

Qualifications:

Minimum of a Ph.D. in Electrical & Computer Engineering or a related field, expertise in the field relevant to the course, and appropriate teaching experience. Previous educational background and/or experience must be suited to teaching the course described below. Candidates must have excellent communication and presentation skills, as well as be capable of working as a member of a teaching team. Prior teaching experience in project-based engineering courses and lecture-based engineering courses would be a strong asset. Preference will be given to candidates who are registered as professional engineers in the province of Ontario.

Teaching requirement:

Winter Term Course: January 1, 2021 – April 30, 2021
Anticipated course enrolment: 40

Course Description

ELEC 470  Computer System Architecture  W3.5

Description

ELEC 470 covers some of the advanced topics in computer architecture with a quantitative perspective. It explores the architectural details that are essential for effective understanding, application, and performance characterization of modern processors, multiprocessors, clusters, and GPU architectures, with hierarchical memory subsystems. This course first studies the fundamentals of quantitative design and analysis, and then introduces the instruction set design through the use of a MIPS instruction set architecture. An important portion of the course is dedicated to exploring processor design and implementation with a focus on instruction level parallelism (ILP), including single-issue pipelined processors, multiple-issue (superscalar) processors, with static and dynamic scheduling and speculation, along with simulation studies. The course then discusses multicore processors and shared-memory multiprocessor architectures, with a focus on thread level parallelism (TLP), cache coherency and parallel programming. It then studies multicore clusters and message passing systems. Hierarchical memory subsystems, including multi-level caches and integration with pipelined processors, and virtual memory with address translation is then covered. Finally, the course discusses data level parallelism (DLP), and GPU architectures.

This course builds on and supplements knowledge from other courses, including ELEC 271, ELEC 274, and ELEC 371 as formal prerequisites, along with ELEC 374 (taken only by Computer Engineering Students) for additional background.
Objectives

- Understand computer performance, power, energy and cost metrics, laws, as well as standard benchmarking techniques to quantitatively design and analyze computer systems.
- Understand the principles of the reduced instruction set design (RISC) architecture through MIPS instruction set architecture (ISA).
- Write and interpret simple code sequences in MIPS assembly language. Understand instruction formats, addressing modes, register usage conventions, and procedure support in MIPS, and translate simple codes in C to MIPS.
- Understand the design of a single-issue, non-pipelined datapath with control unit for the MIPS ISA. Realize how to extend the design for new instructions and features.
- Understand the design of a single-issue, pipelined datapath with control unit for the MIPS ISA. Realize how structural, data and control hazards can affect performance. Understand how data hazards can be handled by code scheduling statically, or by forwarding and/or stalling dynamically in hardware. Understand how techniques such as delay slots or static/dynamic branch prediction can resolve control hazards in pipelined processors. Determine the performance of pipeline with stalls, and understand how to deal with exceptions. Understand how to extend the pipeline to support multi-cycle floating-point operations, and how hazards and forwarding are handled in longer latency pipelines.
- Understand advanced ILP, including multiple-issue pipelined processors with static scheduling (VLIW), dynamic scheduling (superscalar), in-order execution, out-of-order execution, out-of-order execution with speculation, and with in-order commit. Learn scheduling, loop unrolling and register renaming in static multiple-issue MIPS pipeline. Understand true dependency, output dependency, and antidependency. Learn dynamic scheduling with a scoreboard for MIPS, and dynamic scheduling with the Tomasulo’s algorithm. Understand increasing ILP further by extending Tomasulo’s algorithm with hardware based speculation. Study the limitations of ILP for realizable processors. Understand how to use multithreading (MT) to improve superscalar performance: coarse-grained MT, fine-grained MT, and simultaneous MT.
- Understand processor-memory performance gap, and the memory hierarchy as a potential architectural technique to remedy the situation. Understand single-level and multi-level cache architectures, multilevel inclusion vs. multilevel exclusion, cache read and write policies, write-through vs. write-back policies, write buffer, write allocate vs. no-write allocate, split caches vs. a unified cache. Handle cache misses in the pipeline, and understand the impact of cache performance on processor pipeline, miss penalty and out-of-order execution. Learn basic and advanced cache optimization techniques, including non-blocking and multi-banked caches, and hardware vs. compiler-controlled prefetching.
- Understand the memory management unit, virtual memory and virtual-to-physical address translation, and translation look-aside buffer (TLB). Learn cache, virtual memory and TLB integration.
- Use simulation tools to reinforce understanding of pipelining, and the issues involved in pipelining such as data, control and structural hazards. Study how forwarding and code scheduling might remove or reduce the number of stalls due to different kinds of hazards.
- Use simulation tools to obtain dynamic instruction execution statistics and understand the different characteristics of application programs, to understand how branch prediction efficiency affects an application’s performance, to understand the trade-offs among different branch prediction strategies, to compare in-order execution with out-of-order execution and speculation, and to understand the relative importance of various techniques, to have a better understanding of how various cache parameters affects performance, and to understand the trade-offs between different TLB organizations.
- Understand multiprocessor architectures, from symmetric multiprocessors (SMP) to distributed shared memory multiprocessors (DSM), to message passing multiprocessors (clusters, MPPs). Understand challenges in parallel processing (partitioning, communication costs, synchronization cost, scheduling, load balancing, and parallel algorithms), Amdahl’s Law, Gustafson’s Law, and weak scaling vs. strong scaling.
- Understand shared memory multiprocessors, and shared memory programming through examples, process synchronization, lock/unlock mechanisms and hardware primitives in MIPS, spin-lock synchronization, and barriers. Cache coherency and memory consistency problem. Snooping vs.
directory-based cache coherency protocols, write invalidate vs. write update cache coherency, deriving
protocol state transition for MSI, MESI, and MOESI multiprocessor cache coherence protocols, and false
sharing impact. Writing parallel programs using Pthreads and OpenMP on multicore, multiprocessor
nodes. Principles of message passing programming, pros and cons with shared memory programming,
Message Passing Interface (MPI), and mixed-mode programming.

Credit Breakdown
Lecture: 3
Lab: 0
Tutorial: 0.5

Academic Unit Breakdown
Mathematics 0
Natural Sciences 0
Complementary Studies 0
Engineering Science 11
Engineering Design 31

The successful applicant will have 100 percent responsibility for the course and will be required to convert
course materials to an accessible online format satisfactory to the Department Head.

Winter term classes begin 10 January 2022.

Queen’s University is committed to employment equity and diversity in the workplace and welcomes
applications from women, visible minorities, aboriginal people, persons with disabilities, and persons of any
sexual orientation or gender identity. All qualified candidates are encouraged to apply; however, Canadians and
permanent residents of Canada will be given priority. Academic staff at Queen’s University is governed by a
collective agreement between QUFA, QUFA and Queen’s University.

The Queen’s University Policy Regarding Mandatory Vaccination Requirements for In-person University
Activities requires ALL Community Members, including employees, to be Fully Vaccinated against COVID-19
prior to participating in any In-person University Activities. This is a condition of employment for all employees
who are required to attend University Property to perform their employment responsibilities. Individuals who
cannot be vaccinated due to substantiated grounds (medical and other protected grounds under the Ontario
Human Rights Code) may ask the University to validate the exemption and request an accommodation for
these rare circumstances. If approved, they will be subject to additional health and safety measures.

The University will provide support in its recruitment processes to applicants with disabilities, including
accommodation that takes into account an applicant’s accessibility needs. If you require accommodation during
the interview process, please contact Mary Gillespie, mary.gillespie@queensu.ca.

To comply with Federal laws, the University is obliged to gather statistical information about how many
applicants for each job vacancy are Canadian citizens/ permanent residents of Canada. Applicants need not
identify their country of origin or citizenship, however, all applications must include one of the following
statements: I am a Canadian citizen/permanent resident of Canada; OR, I am not a Canadian
citizen/permanent resident of Canada. Applications that do not include this information will be deemed
incomplete.

Applications should include a complete and current curriculum vitae, a statement of teaching experience, the
names and contact details of two referees who may be contacted, and any relevant other materials the
candidate wishes to submit for consideration. Applications can be submitted to the ECE Appointments Committee at the address below, or by email to Mary Gillespie at mary.gillespie@queensu.ca. Applications should be received no later than November 12, 2021.

Electrical and Computer Engineering Appointments Committee  
C/o Mary Gillespie, Administrative Assistant  
Department of Electrical and Computer Engineering  
Walter Light Hall, Room 416  
19 Union Street  
Queen’s University  
Kingston, ON  K7L 3N6  
Tel.:  613-533-6000 ext.75344  
Fax: 613-533-6615