The Department of Electrical and Computer Engineering in the Faculty of Engineering and Applied Science at Queen’s University requests applications from suitably qualified candidates interested in teaching the following undergraduate course in the 2021-22 session.

Qualifications:

Minimum of a Ph.D. in Electrical & Computer Engineering or a related field, expertise in the field relevant to the course, and appropriate teaching experience. Previous educational background and/or experience must be suited to teaching the course described below. Candidates must have excellent communication and presentation skills, as well as be capable of working as a member of a teaching team. Prior teaching experience in project-based engineering courses and lecture-based engineering courses would be a strong asset. Preference will be given to candidates who are registered as professional engineers in the province of Ontario.

Teaching requirement:

Winter Term Course: January 1, 2021 – April 30, 2021
Anticipated course enrolment: 160

Course Description

ELEC 274 Computer Architecture W4

Description

This course provides an introduction to basic computer structure, instruction set architecture, assembly-language programming, input/output considerations, processor design based on digital logic, and memory technology and memory system design principles. The primary intent is to provide a foundation for subsequent courses on hardware/software interfacing for microprocessor-based systems, computer system architecture, and digital systems engineering. A secondary intent is to provide an appreciation of the low-level representation of software compiled from high-level languages into machine instructions. The practical aspects of the course are illustrated with the 32-bit Altera Nios II instruction set architecture and soft processor for implementation in field-programmable logic chips, but the principles that are conveyed using this example are largely applicable to any instruction set architecture and processor implementation. This course builds on and supplements knowledge from other courses on digital logic, circuits and electronics, and software/programming.

Course Learning Outcomes (CLOs)

- Understand the basic functional units in a typical computer system.
- Understand binary number representation including two's-complement signed values, hexadecimal number representation, and character representation using the ASCII encoding.
- Understand the common basic features of a processor, including the program counter register, instruction register, general-purpose registers, and memory interface.
• Describe the essential steps for fetching, decoding, and executing instructions with respect to the common basic features of a processor.
• Understand memory organization concepts, including endian-ness and byte addressability.
• Understand assembly-language instruction syntax including mnemonics, operand specification, and addressing modes.
• Understand subroutine linkage, the use of the processor stack, and subroutine nesting.
• Design and implement assembly-language programs by interpreting specifications, partitioning the computation into tasks, defining data structures, organizing subroutines, preparing pseudocode specifications for subroutines, and translating the pseudocode into assembly language.
• Understand basic input/output interfaces and assembly-language implementation of program-controlled input/output operations.
• Understand the partition of instruction processing into basic steps that correspond to stages of execution in hardware.
• Understand the design of the control portion of a processor, and its datapath consisting of the general-purpose register file, the arithmetic/logic unit, the memory interface, internal registers between stages, and multiplexers for selecting inputs to components.
• Understand the common organizational and operational characteristics of semiconductor-based memory components.
• Distinguish between different memory implementation technologies such as SRAM, DRAM, and EEPROM (including Flash type).
• Understand hierarchical memory design with caches, main memory, and secondary storage.
• Understand cache organization, mapping functions, and the role of temporal and spatial locality in program execution in dictating performance with caches.
• Design caches from given specifications on total capacity, block size, and mapping function.
• Understand the concept of virtual memory, relevant hardware support for it, and its basic operation.

Credit Breakdown
Lecture: 3
Lab: 0.5
Tutorial: 0.5

Academic Unit Breakdown

Mathematics 0
Natural Sciences 0
Complementary Studies 0
Engineering Science 26
Engineering Design 22

The successful applicant will have 100 percent responsibility for the course and will be required to convert course materials to an accessible online format satisfactory to the Department Head.

Winter term classes begin 10 January 2022.

The University invites applications from all qualified individuals. Queen’s is strongly committed to employment equity, diversity, and inclusion in the workplace and encourages applications from Black, racialized/visible minority and Indigenous/Aboriginal people, women, persons with disabilities, and 2SLGBTQ+ persons. All qualified candidates are encouraged to apply; however, Canadians and permanent residents of Canada will be given priority. Academic staff at Queen’s University is governed by a collective agreement between QUFA and Queen’s University.

The University will provide support in its recruitment processes to applicants with disabilities, including accommodation that takes into account an applicant’s accessibility needs. If you require accommodation during the interview process, please contact Mary Gillespie, mary.gillespie@queensu.ca.
The Queen’s University Policy Regarding Mandatory Vaccination Requirements for In-person University Activities requires ALL Community Members, including employees, to be Fully Vaccinated against COVID-19 prior to participating in any In-person University Activities. This is a condition of employment for all employees who are required to attend University Property to perform their employment responsibilities. Individuals who cannot be vaccinated due to substantiated grounds (medical and other protected grounds under the Ontario Human Rights Code) may ask the University to validate the exemption and request an accommodation for these rare circumstances. If approved, they will be subject to additional health and safety measures.

To comply with Federal laws, the University is obliged to gather statistical information about how many applicants for each job vacancy are Canadian citizens/permanent residents of Canada. Applicants need not identify their country of origin or citizenship, however, all applications must include one of the following statements: I am a Canadian citizen/permanent resident of Canada; OR, I am not a Canadian citizen/permanent resident of Canada. Applications that do not include this information will be deemed incomplete.

Applications should include a complete and current curriculum vitae, a statement of teaching experience, the names and contact details of two referees who may be contacted, and any relevant other materials the candidate wishes to submit for consideration. Applications can be submitted to the ECE Appointments Committee at the address below, or by email to Mary Gillespie at mary.gillespie@queensu.ca. Applications should be received no later than November 12, 2021.

Electrical and Computer Engineering Appointments Committee
C/o Mary Gillespie, Administrative Assistant
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